A Generic and Compositional Framework for Multicore Response Time Analysis

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ABSTRACT

In this paper, we introduce a Multicore Response Time Analysis (MRTA) framework. This framework is extensible to different multicore architectures, with various types and arrangements of local memory, and different arbitration policies for the common interconnects. We instantiate the framework for single level local data and instruction memories (cache or scratchpads), for a variety of memory bus arbitration policies, including: Round-Robin, FIFO, Fixed-Priority, Processor-Priority, and TDMA, and account for DRAM refreshes. The MRTA framework provides a general approach to timing verification for multicore systems that is parametric in the hardware configuration and so can be used at the architectural design stage to compare the guaranteed levels of performance that can be obtained with different hardware configurations. The MRTA framework decouples response time analysis from a reliance on context independent WCET values. Instead, the analysis formulates response times directly from the demands on different hardware resources.

1. INTRODUCTION

Effective analysis of the worst-case timing behaviour of systems built on multicore architectures is essential if these high performance platforms are to be deployed in critical real-time embedded systems used in the automotive and aerospace industries. We identify four different approaches to solving the problem of determining timing correctness.

With single core systems, a traditional two-step approach is typically used. This consists of timing analysis which determines the context-independent worst-case execution time (WCET) of each task, followed by schedulability analysis, which uses task WCETs and information about the processor scheduling policy to determine if each task can be guaranteed to meet its deadline. When local memory (e.g. cache) is present, then this approach can be augmented by analysis of Cache Related Pre-emption Delays (CRPD) [4], or by partitioning the cache to avoid CRPD altogether. Both approaches are effective and result in tight upper bounds on task response times [5].

With a multicore system, the situation is more complex since WCETs are strongly dependent on the amount of cross-core interference on shared hardware resources such as main memory, L2-caches, and common interconnects, due to tasks running on other cores. The uncertainty and variability in this cross-core interference renders the traditional two-step process ineffective for many multicore processors. For example, on the Freescale P4080, the latency of a read operation varies from 40 to 600 cycles depending on the total number of cores running and the number of competing tasks [32]. Similarly, a 14 times slowdown has been reported [35] due to interference on the L2-cache for tasks running on Intel Core 2 Quad processors.

At the other extreme is a fully integrated approach. This involves considering the precise interleaving of instructions originating from different cores [19]; however, such an approach suffers from potentially insurmountable problems of combinatorial complexity, due to the proliferation of different path combinations, as well as different release times and schedules.

An alternative approach is based on temporal isolation [14]. The idea here is to statically partition the use of shared resources, e.g. space partitioning of cache and DRAM banks, time partitioning of bus access, so that context-independent WCET values can be used and the traditional two-step process applied. This approach raises a further challenge, how to partition the resources to obtain schedulability [36]. Techniques which seek to limit the worst-case cross-core interference, for example by using TDMA arbitration on the memory bus or by limiting the amount of contention by suspending execution on certain cores [32], can have a significant detrimental effect on performance, effectively negating the performance benefits of using a multicore system altogether. We note that TDMA is rarely if ever used as a bus-arbitration policy in real multicore processors, since it is not work-conserving and so wastes significant bandwidth. This impacts both worst-case and average-case performance; essential for application areas such as telecommunications, which have a major influence on processor design.

The final approach is the one presented in this paper, based on explicit interference modelling. We explore the premise that due to the strong interdependencies between timing analysis and schedulability analysis on multicore systems, they need to be considered together. In our approach, we omit the notion of WCET per se and instead directly target the calculation of task response times.

In this work, we use execution traces to model the behaviour of tasks. Traces provide a simple yet expressive way to model task behaviour. Note that relying on execution traces does not pose a fundamental limitation to our approach as all required performance quantities can also be derived using static analysis [28, 17, 1] as within the traditional context-independent timing analysis; however, traces enable a near-trivial static cache...
analysis and so allow us to focus on response time analysis.

The main performance metrics are the processor demand and the memory demand of each task. The latter quantity feeds into analysis of the arbitration policy used by the common interconnect, enabling us to upper bound the total memory access delays which may occur during the response time of the task. By computing the overall processor demand and memory demand over a relatively long interval of time (i.e. the task response time), as opposed to summing the worst case over many short intervals (e.g. individual memory accesses), we are able to obtain much tighter response time bounds. The Multicore Response Time Analysis framework (MRTA) that we present is extensible to different types and arrangements of local memory, and different arbitration policies for the common interconnect. In this paper, we instantiate the MRTA framework assuming the local memories used for instructions and data are single-level and either cache, scratchpad, or not present. Further, we assume that the memory bus arbitration policy may be TDMA, FIFO, Round-Robin, or Fixed-Priority (based on task priorities), or Processor-Priority. We also account for the effects of DRAM refresh [6, 11]. The general approach embodied in the MRTA framework is extensible to more complex, multi-level memory hierarchies, and other sources of interference. It provides a general timing verification framework that is parametric in the hardware configuration (common interconnect, local memories, number of cores etc.) and so can be used at the architectural design stage to compare the guaranteed levels of performance that can be obtained with different hardware configurations, and also during the development and integration stages to verify the timing behaviour of a specific system.

While the specific hardware models and their mathematical representations used in this paper cannot capture all of the interference and complexity of actual hardware, they serve as a valid starting point. They include the dominant sources of interference and represent current architectures reasonably well.

2. RELATED WORK

In 2007, Rosen et al. [37] proposed an implementation in which TDMA slots on the bus are statically allocated to cores. This technique relies on the availability of a user-programmable table-driven bus arbiter, which is typically not available in real hardware, and on knowledge at design time, of the characteristics of the entire workload that executes on each core. Chattopadhyay et al. [15] and Kelter et al. [22] proposed an analysis which takes into account a shared bus and instruction cache, assuming separate buses and memories for both code and data (uncommon in real hardware) and TDMA bus arbitration. The method has a limited applicability as it does not address data accesses to memory.

In 2010, Schranzhofer et al. [39] developed a framework for analysing the worst-case response time of real-time tasks on a multi core with TDMA arbitration. This was followed by work on resource adaptive arbiters [40]. They proposed a task model in which tasks consist of sequences of super-blocks, themselves divided into phases that represent implicit communication (fetching or writing of data from/to memory), computation (processing the data), or both. Contrary to the technique presented here, their approach requires major program intervention and compiler assistance to prefetch data.

Also in 2010, Lv et al. [30] proposed a method to model request patterns and the memory bus using timed automata. Their method handles instruction accesses only and may suffer from state-space explosion when applied to data accesses. A method employing timed automata was proposed by Gustavsson et al. [19] in which the WCET is obtained by proving special predicates through model checking. This approach allows for a detailed system modelling but is also prone to the state-space explosion problem. In 2014, Kelter et al. [23] analysed the maximum bus arbitration delays for multiprocessor systems sharing a TDMA bus and using both (private) L1 and (shared) L2 instruction and data caches.

Pellizzoni et al. [34] compute an upper bound on the contention delay incurred by periodic tasks, for systems comprising any number of cores and peripheral buses sharing a single main memory. Their method does not cater for non-periodic tasks and does not apply to systems with shared caches. In addition it relies on accurate profiling of cache utilization, suitable assignment of the TDMA time-slots to the tasks’ super-blocks, and imposes a restriction on where the tasks can be pre-empted.

Schliecker et al. [38] proposed a method that employs a general event-based model to estimate the maximum load on a shared resource. This approach makes very few assumptions about the task model and is thus quite generally applicable. However, it only supports a single unspecified work-conserving bus arbiter.

Paolieri et al. [33] proposed a hardware platform that enforces a constant upper bound on the latency of each access to a shared resource. This approach enables the analysis of tasks in isolation since the interference on other tasks can be conservatively accounted for using this bound. Similarly, the PTARM [29] enforces constant latencies for all instructions, including loads and stores. However, both cases represent customized hardware.

Kim et al. [24] presented a model to upper bound the memory interference delay caused by concurrent accesses to a shared DRAM main memory. Their work differs from this paper in that they do not assume a unique shared bus to access the main memory and they primarily focus on the contention at the DRAM controller by assuming a fully partitioned private and shared cache model. (For shared caches they assume that the extra number of requests generated due to cache line evictions at runtime is given).

Yun et al. [42] proposed a software-based memory throttling mechanism to explicitly limit the memory request rate of each core and thereby control the memory interference. They also developed analytical solutions to compute proper throttling parameters that satisfy schedulability of critical tasks while minimising the performance impact of throttling.

In 2015, Dasari et al. [16] proposed a general framework to compute the maximum interference caused by the shared memory bus and its impact on the execution time of the tasks running on the cores. The method in [16] is more complex than that proposed in this paper, and may be more accurate when it estimates the delay due to the shared bus, but it does not take cache-related effects into account (by assuming partitioned caches), which makes it less generic than the framework proposed here.

Regarding shared caches, Yan and Zhang [41] addressed the problem of computing the WCET of tasks assuming direct-mapped, shared L2 instruction caches on multicores. The applicability of the approach is unfortunately limited as it makes very restrictive assumptions such as (1) data caches are perfect, i.e. all accesses are hits, and (2) data references from different threads will not interfere with each other in the shared L2 cache. Li et al. [27] proposed a method to estimate the worst-case response time of concurrent programs running on multicores with shared L2 caches, assuming set-associative instruction caches using the LRU replacement policy. Their work was later extended [15] by adding a TDMA bus analysis technique to bound the memory access delay.

3. SYSTEM MODEL

In this paper, we provide a theoretical framework that can be instantiated for a range of different multicore architectures with different types of memory hierarchy and different arbitration policies for the common interconnect. Our aim is to create a flexible, adaptable, and generic analysis framework wherein a large number of common multicore architecture designs can be modeled and analysed. In this paper inevitably we can only cover
a limited number of types of local memory, bus, and global memory behaviour. We select common approaches to model the different hardware components and integrate them into an extensible framework.

### 3.1 Multicore Architectural Model

We model a generic multicore platform with \( \ell \) timing-compositional cores \( P_1, \ldots, P_\ell \) as depicted in Figure 1. By timing-compositional cores we mean cores where it is safe to separately account for delays from different sources, such as computation on a given core and interference on a shared bus [20].

The set of cores is defined as \( \mathbb{P} \). Each core has a local memory which is connected via a shared bus to a global memory and IO interface. We assume constant delays \( d_{\text{mem}} \) to retrieve data from global memory under the assumption of an instantaneous bus access, i.e., no wait-cycles or contention on the bus. We assume atomic bus transactions, i.e., no split transactions, which furthermore are not re-ordered, and non-preemptable busy waiting on the processor for requests to be serviced. Further, we assume that bus access may be given to cores for one access at a time. The types of the memories and the bus policy are parameters that can be instantiated to model different multicore systems. In this paper, we omit a consideration of delays due to cache coherence and synchronization, and we assume write-through caches only. Write-back caches are discussed in technical report [2].

![Multicore Platform](image1)

*Figure 1: Multicore Platform. A set of \( \ell \) processors with local memories connected via a common bus to a global memory.*

#### 3.2 Task Model

We assume a set of \( n \) sporadic tasks \( \{\tau_1, \ldots, \tau_n\} \), each task \( \tau_i \) has a minimum period or inter-arrival time \( T_i \) and a deadline \( D_i \). Deadlines are assumed to be constrained, hence \( D_i \leq T_i \).

We assume that the tasks are statically partitioned to the set of \( \ell \) identical cores \( \{P_1, \ldots, P_\ell\} \), and scheduled on each core using fixed-priority pre-emptive scheduling. The set of tasks assigned to core \( P_i \) is denoted by \( \Gamma_i \).

The index of each task is unique and thus provides a global priority order, with \( \tau_1 \) having the highest priority and \( \tau_n \) the lowest. The global priority of each task translates to a local priority order on each core which is used for scheduling purposes. We use \( \text{hp}(i) \) (\( \text{lp}(i) \)) to denote the set of tasks with higher (lower) priority than that of task \( \tau_i \), and we use \( \text{hp}(i) \) (\( \text{lp}(i) \)) to denote the set of tasks with higher or equal (lower or equal) priority to task \( \tau_i \).

We initially assume that the tasks are independent, in so far as they do not share mutually exclusive software resources (discussed in the technical report [2]); nevertheless, the tasks compete for hardware resources such as the processor, memory, and the bus.

The execution of task \( \tau_i \) is modelled using a set of traces \( \mathcal{O}_i \), where each trace \( o = [o_1, \ldots, o_t] \) is an ordered list of instructions. For ease of notation, we treat the ordered list of instructions as a multi-set, whenever we can abstract away from the specific order.

We distinguish three types of instructions \( it \):

\[
\begin{align*}
    it = \begin{cases} 
    r[m^d] & \text{read data from memory block } m^d \\
    w[m^d] & \text{write data to memory block } m^d \\
    e & \text{execute}
    \end{cases}
\end{align*}
\]  

(1)

An instruction \( \iota \) is a triple consisting of the instruction’s memory address \( m^\iota \), its execution time \( \Delta \) without memory delays, i.e., assuming a perfect local memory, and the instruction type \( it \):

\[
\iota = (m^\iota, \Delta, it)
\]  

(2)

The set of memory blocks is denoted as \( M \). \( M^{da} \) denotes the data memory blocks, \( M^m \) the instruction memory blocks. We assume that data and instruction memory are disjoint, i.e., \( M^m \cap M^{da} = \emptyset \).

The use of traces to model a task’s behaviour is unusual as the number of traces is exponential in the number of control-flow branches. Despite this obvious drawback, traces provide a simple yet expressive way to model task behaviour. They enable a near-trivial static cache analysis and a simple multicore simulation to evaluate the accuracy of the timing verification framework. However, most importantly, traces show that the worst-case execution behaviour of a task \( \tau_i \) on a multicore system is not uniquely defined. From the viewpoint of a task scheduled on the same core, \( \tau_i \) may have the highest impact when it uses the core for the longest possible time interval, whereas the impact on tasks scheduled on any other core may be maximized when \( \tau_i \) produces the largest number of bus accesses. These two cases may well correspond to different execution traces. As a remedy for the exponential number of traces, the complexity can be reduced by (i) computing a synthetic worst-case trace or (ii) by deriving the set of Pareto optimal traces that maximize the task’s impact according to a predefined cost function (see [28]). We can also completely resort to static analysis to derive upper bounds on the performance metrics. Static analyses provide independent upper bounds on the different performance quantities. This strongly reduces the computational complexity, but may lead to pessimism.

An evaluation of this trade-off is future work.

### 4. MEMORY MODELLING

In this section we show how the effects of a local memory can be modelled via a \( \text{MEM} \) function which describes the number of accesses due to a task which are passed to the next level of the memory hierarchy, in this case main memory. The \( \text{MEM} \) function is instantiated for both cache and scratchpads. We model the effect of a (local) memory using a function of the form:

\[
\text{MEM}: \emptyset \to \mathbb{N} \times 2^{2^n} \times 2^{2^n}
\]  

(3)

where \( \text{MEM}(o) = (M^\Delta_o, UC^O_o, ECB^O_o) \) computes, for a trace \( o \), the number of bus accesses i.e., the number of memory accesses which cannot be served by the local memory alone (denoted as memory demand \( MD \)), \( UC^O_o \) denotes a multiset containing, for each program point in trace \( o \), the set of Useful Cache Blocks (UCBs) [25], which may need to be reloaded when trace \( o \) is pre-empted at that program point, and the set of Evicting Cache Blocks (ECBs) which is the set of all cache blocks accessed by trace \( o \) which may evict memory blocks of other tasks. The value MD does not just cover cache misses, but also has to account for write accesses. In the case of write-through caches, each write access will cause a bus access, irrespective of whether or not the memory block is present in cache.

The number of bus accesses MD assumes non-preemptive execution. With pre-emptive execution and caches, more than MD memory accesses can contribute to the bus contention due to cache eviction. In this paper, we make use of the CRPD analysis for fixed-priority pre-emptive scheduling introduced in [4].

We now derive instantiations of the function \( \text{MEM}(o) \) for a trace \( o = [o_1, \ldots, o_t] \) for instruction memories and data memories for systems (i) without cache, (ii) with scratchpads, and (iii) with direct-mapped or LRU caches. In the following, the superscripts indicate data \( (da) \) or instruction memory \( (in) \), the subscripts the type of memory, i.e., uncached \( (uc) \), scratchpad \( (sp) \), or caches \( (c) \).
4.1 Uncached

Considering instruction memory, the number of bus accesses for a system with no cache is given by the number of instructions $k$ in the trace. The set of UCBs and ECBs are empty. Pre-emption has no effect on the local memory, since none exists.

$$\text{MEM}^{\text{uc}}(o) = (k, 0, 0)$$ (4)

Considering data memory, we have to account for the number of data accesses, irrespective of read or write access. The number of accesses is thus equal to the number of data access instructions.

$$\text{MEM}^{\text{da}}(o) = \left| \{t_i | t_i \in o \land t_i = (_{\_ \_ \_ \_}, r/w[m^d])\} \right|, 0, 0$$ (5)

4.2 Scratchpads

A scratchpad memory is defined using a function $\text{SPM}: \mathbb{M} \rightarrow \{true, false\}$, which returns true for memory blocks that are not changed in the scratchpad. For ease of presentation, we assume a static a write-through scratchpad configuration, which does not change at runtime. An extension to dynamic scratchpads and the write-back policy is straightforward, but beyond the scope of this paper.

Each memory access to a memory block which is not stored in the scratchpad causes an additional bus access.

$$\text{MEM}^{\text{sp}}(o) = \left| \{m^i | (m^i,_{\_ \_ \_ \_} \in o \land \neg \text{SPM}(m^i))\} \right|, 0, 0$$ (6)

Further, in the case of write accesses, even if a memory block is stored in the scratchpad, that access also contributes to the bus contention as we assume a write-through policy.

$$\text{MEM}^{\text{sp}}(o) = \left| \{m^d | (((_{\_ \_ \_ \_}, r(m^d)) \in o \land \neg \text{SPM}(m^d))\} \right|, 0, 0$$ (7)

The sets of UCBs and ECBs are empty as no pre-emption overhead is assumed with static scratchpad memory. Dynamic scratchpad management is discussed in the technical report [2].

4.3 Caches

We assume a function $\text{Hit}: \mathbb{I} \times \mathbb{M} \rightarrow \{true, false\}$, which classifies each memory access at each instruction as a cache hit or a cache miss. This function can be derived using cache simulation of the trace starting with an empty cache or by using traditional cache analysis [17], where each unclassified memory access is considered a cache miss. This means that we upper bound the number of cache misses. For each possible pre-emption point $t$ on trace $o$, the set of UCBs is derived using the corresponding analysis described in Altmeyer’s thesis [1], Chapter 5, Section 4. It is sufficient to only store the cache sets a useful memory blocks maps to, instead of the useful memory blocks. The multiset $\overline{\text{UCB}}_o$ then contains, for each program point $t$ in trace $o$, the set of UCBs at that program point, i.e., $\overline{\text{UCB}}_o = \bigcup_{t \in o} \overline{\text{UCB}}_t$. The set of ECBs is the set of all cache sets of memory blocks on trace $o$.

$$\text{MEM}^{\text{sp}}(o) = \left| \{m^i | (m^i,_{\_ \_ \_ \_} \in o \land \neg \text{Hit}(m^i, t_i))\} \right|, \overline{\text{UCB}}_o, \text{ECB}^i$$ (8)

Since we assume a write-through policy, write accesses contribute to the cache contention and have to be treated accordingly.

$$\text{MEM}^{\text{sp}}(o) = \left| \{m^d | ((_{\_ \_ \_ \_}, r(m^d)) \in o \land \neg \text{Hit}(m^d, t_i))\} \right|, \overline{\text{UCB}}_o, \text{ECB}^d$$ (9)

4.4 Memory Combinations

To allow different combinations of local memories, for example scratchpad memory for instructions and an LRU cache for data, we define the combination of instruction memory $\text{MEM}^{\text{in}}$ and data memory $\text{MEM}^{\text{da}}$ as follows.

$$\text{MEM}(o) = \left( MD^i_o + MD^d_o, \overline{\text{UCB}}^i_o, \text{ECB}^i_o \right)$$ (10)

with $\text{MEM}(o) = \left( MD^i_o, \overline{\text{UCB}}^i_o, \text{ECB}^i_o \right)$ being the result for the instruction memory and $\text{MEM}(o) = \left( MD^d_o, \overline{\text{UCB}}^d_o, \text{ECB}^d_o \right)$ for the data memory.

5. BUS MODELLING

In this section we show how the memory bus delays experienced by a task can be modelled via a bus function of the form:

$$\text{BUS}: \mathbb{N} \times \mathbb{P} \times \mathbb{N} \rightarrow \mathbb{N}$$ (11)

where $\text{BUS}(i, x, t)$ determines an upper bound on the number of bus accesses that can delay task $t$, on processor $P$, during a time interval of length $t$. This abstraction covers a variety of bus arbitration policies, including Round-Robin, FIFO, Fixed-Priority, and Processor-Priority, all of which are work-conserving, and also TDMA which is not work-conserving.

We now introduce the mathematical representations of the delays incurred under these arbitration policies. We note that the framework is extensible to a wide variety of different policies. The only constraints we place on instantiations of the $\text{BUS}(i, x, t)$ function is that they are monotonically non-decreasing in $t$.

Let $\tau_i$ be the task of interest, and $x$ the index of the processor $P$, on which it executes. Other task indices are represented by $j, k$ etc., while $y, z$ are used for processor indices.

Let $S_i^y(t)$ denote an upper bound on the number of bus accesses due to $\tau_i$, and all higher priority tasks that run on processor $P$, during an interval of length $t$. Let $A_i^y(t)$ be an upper bound on the number of bus accesses due to all tasks of priority $j$ or higher executing on some processor $P, t < P$, during an interval of length $t$ (note, $j$ may not necessarily be the priority of a task allocated to processor $P$).

As memory bus requests are typically non-preemptive, one lower priority memory request may block a higher priority one, since the global, shared memory may have just received a lower priority request before the higher priority one arrives. To account for these blocking accesses, we use $L_i^y(t)$ which denotes an upper bound on the total number of bus accesses due to all tasks of priority lower than $j$ executing on some other processor $P, t < P$, during an interval of length $t$. In Section 6 we show how the values of $S_i^y(t)$, $A_i^y(t)$ and $L_i^y(t)$ are computed and explain why $S_i^y(t)$ and $A_i^y(t)$ are subtly different and hence require distinct notation.

In the following equations for the $\text{BUS}(i, x, t)$ function, we account for blocking due to one non-preemptive access from lower priority tasks running on the same core $P$, as task $\tau_i$ (i.e. $x = 1$ in the equations). This holds because such blocking can only occur at the start of the the priority level-$i$ (processor) busy period.

For a Fixed-Priority bus with memory accesses inheriting the priority of the task that generates them, we have:

$$\text{BUS}(i, x, t) = S_i^y(t) + \sum_{y \neq x} A_i^y(t) + \min \left( S_i^y(t), \sum_{y \neq x} L_i^y(t) \right) + 1$$ (12)

1Here we mean priorities on the bus, which are not necessarily the same as task priorities.
The term min \( \sum_{x \in x} A_x(t) \) upper bounds the blocking due to tasks of lower priority than \( \tau \) running on other cores.

For a Processor-Priority bus with memory accesses inheriting the priority of the core rather than the task, we have:

\[
BUS(i, x, t) = S^i(t) + \sum_{y \neq x} A_y(t) + \min \left( S^i(t), \sum_{y \neq x} A_y(t) \right) + 1
\]

where \( HP(x) \) (LP(x)) is the set of processes with higher (lower) priority than that of \( P_x \), and \( n \) is the index of the task with the lowest priority. The term \( A_y(t) \) thus captures the interference of all tasks running on processor \( y \), independent of their priority, and the term \( \sum_{y \neq x} A_y(t) \) upper bounds the blocking due to tasks running on processors with priority lower than that of \( P_x \).

For a FIFO bus, we assume that all accesses generated on the other processors may be serviced ahead of the last access of \( \tau \), hence we have:

\[
BUS(i, x, t) = S^i(t) + \sum_{y \neq x} A_y(t) + 1
\]

Note accesses from other cores do not contribute blocking since we already pessimistically account for all these accesses in the summation term.

For a Round-Robin bus with a cycle consisting of an equal number of slots \( v \) per processor, we have:

\[
BUS(i, x, t) = S^i(t) + \sum_{y \neq x} \min(A_y(t), v \cdot S^i(t)) + 1
\]

The worst-case situation occurs when each access in \( S^i(t) \) is delayed by each core \( P_x \), and \( v \) is the number of accesses from core \( P_x \). Again, as we already account for all accesses from all other cores, there is no separate contribution to blocking. Note unlike TDMA, Round-Robin moves to the next slot immediately if a processor has no access pending.

For a TDMA bus with \( v \) adjacent slots per core in a cycle of length \( \ell \cdot v \), we have:

\[
BUS(i, x, t) = S^i(t) + ((\ell - 1) \cdot v) \cdot S^i(t) + 1
\]

Since TDMA is not work-conserving, the worst case corresponds to each access in \( S^i(t) \) just missing a slot for processor \( P_x \) and hence having to wait at most \((\ell - 1) \cdot v + 1\) slots to be serviced. Effectively, there is additional interference from \((\ell - 1) \cdot v\) slots reserved for other processors on each access, irrespective of whether these slots are used or not. As all accesses due to higher priority tasks on \( P_x \) may be serviced prior to the last access of task \( \tau \), we require \( S^i(t) \) accesses in total to be serviced for \( P_x \). Note that when \( v = 1 \), Equation (16) simplifies to \( BUS(i, x, t) = \ell \cdot S^i(t) + 1 \).

It is interesting to note that while TDMA provides more predictable behaviour, this is at a cost of significantly worse guaranteed performance over long time intervals (e.g. the response time of a task) due to the fact that it is not work-conserving. Effectively, this means that the memory accesses of a task may suffer additional interference due to empty slots on the bus. Nevertheless, Round-Robin behaves like TDMA when all other cores create a large number of competing memory accesses.

We note that the equal number of slots per core for Round-Robin and TDMA, and the grouping of slots per core are simplifying assumptions to exemplify how TDMA and Round-Robin buses can be analysed. An analysis for more complex configurations is reserved for future work.

6. RESPONSE TIME ANALYSIS

In this section, we present the centre point of our timing verification framework: interference-aware Multicore Response Time Analysis (MRTA). This analysis integrates the processor and memory demands of the task of interest and higher priority tasks running on the same processor, including CRPD. It also accounts for the cross-core interference on the memory bus due to tasks running on the other processors.

A task set is deemed schedulable, if for each task \( \tau \), the response time \( R_{\tau} \) is less than or equal to its deadline \( D_{\tau} \):

\[
\forall \tau : R_{\tau} \leq D_{\tau} \Rightarrow \text{schedulable}
\]

The traditional response time calculation [7] [21] for fixed-priority pre-emptive scheduling on a uniprocessor is based on an upper bound on the WCET of each task \( \tau \), denoted by \( C_{\tau} \). By contrast, our MRTA framework dissects the individual components (processor and memory demands) that contribute to the WCET bound and re-assembles them at the level of the worst-case response time. It thus avoids the over-approximation inherent in using context-independent WCET bounds.

In the following, we assume that \( \tau \) is the task of interest whose schedulability we are checking, and \( P_x \) is the processor on which it runs. Recall that there is a unique global ordering of task priorities even though the scheduling is partitioned with a fixed-priority pre-emptive scheduler on each processor.

6.1 Interference on the Core

We compute the maximal processor demand \( PD_\tau \) for each task \( \tau \) as follows:

\[
PD_\tau = \max_{o \in O} \sum_{x \in x} A_x(t) \Delta
\]

where \( \Delta \) is the execution time of an instruction without memory delays. Task \( \tau \) suffers interference \( I^{PROC}(i, x, t) \) on its core \( P_x \) due to tasks of higher priority running on the same core within a time interval of length \( t \) starting from the critical instant:

\[
I^{PROC}(i, x, t) = \sum_{j \in \Gamma \cup hpi(i)} \left( \sum_{x \in x} A_x(t) \right) \cdot PD_j
\]

6.2 Interference on the local memory

Local memory improves a task’s execution time by reducing the number of accesses to main memory. The memory demand of a trace gives the number of accesses that go to main memory and hence the bus, despite the presence of the local memory. The maximal memory demand \( MD_i \) of a task \( \tau \) is defined by the maximum number of bus accesses of any of its traces:

\[
MD_i = \max_{o \in O} \left( MD_i \left( MEM(o) = (\_, \_, \ldots) \right) \right)
\]

Note that the maximal memory demand refers to the demand of the combined instruction and data memory as defined in Equation (10).

The memory demand \( MD_i \) is derived assuming non-preemptive execution, i.e. that the task runs to completion without interference on the local memory. The sets of UCBs and ECBs are used to compute the additional overhead due to pre-emption. In the computation of this overhead, we use the sets of UCBs per trace \( o \) to preserve precision,

\[
UCB_o = UCB \ \text{with} \ \text{MEM}(o) = (\_, \_, \ldots)
\]

and derive the maximal set of ECBs per task \( \tau \) as the union of the ECBs on all traces.

\[
ECB_i = \bigcup_{o \in O} \left( ECB \left| MEM(o) = (\_, \_, \ldots) \right. \right)
\]

We use \( \gamma_{i,j} \) (with \( j \in hpi(i) \)) to denote the overhead (additional accesses) due to a pre-emption of task \( \tau \) by task \( \tau \) on core \( P_x \). We use the ECB-Union [3] approach as an exemplar of CRPD...
analysis, as it provides a reasonably precise bound on the pre-emption overhead with low complexity. Other techniques [4] [26] could also be integrated into this framework, but we omit the explanation due to space constraints. The ECB-Union approach considers the UCBs of the pre-empted task per pre-emption point and assumes that the pre-empting task \( \tau_k \) has already been pre-empted by all tasks with higher priority on the same processor \( P_i \). This nested pre-emption of the pre-empting task is represented by the union of the UCBS of all tasks with higher or equal priority than task \( \tau_k \) (see [4] for a detailed description).

\[
\gamma_{i,j,k} = \max_{t \in \text{lechep}(j)} \left( \max_{o \in \text{oecp}(j)} \text{UCB}(i, o, j) \cup \text{ECB}(i, k) \right)
\]

(22)

### 6.3 Interference on the Bus

We now compute the number of accesses that compete for the bus during a time interval of length \( t \), equating to the worst-case response time of the task of interest \( \tau_k \). We use \( S^i_j(t) \) to denote an upper bound on the total number of bus accesses that can occur due to tasks running on processor \( P_i \) during that time. Since lower priority tasks cannot execute on \( P_i \) during the response time of task \( \tau_k \) (a priority level-\( i \) processor busy period), the only contribution from those tasks is a single blocking access as discussed in Section 5. The maximum delay is computed assuming task \( \tau_k \) is released simultaneously with all higher priority tasks that run on \( P_i \), and subsequent releases of those tasks occur as soon as possible, while also assuming that the maximum possible number of preemptions occur.

\[
S^i_j(t) = \sum_{k \in \text{lechep}(j)} \left[ \frac{t}{T_k} \right] (MD_k + \gamma_{i,k,j})
\]

(23)

\( MD_k \) denotes the memory demand of task \( \tau_k \) and \( \gamma_{i,k,j} \) accounts for the pre-emption costs on core \( P_i \) due to jobs of task \( \tau_k \).

We use \( A^i_j(t) \) to denote an upper bound on the total number of bus accesses due to all tasks of priority \( j \) or higher executing on processor \( P_i \neq P_j \) during an interval of length \( t \). A special case is \( A^i_j(t) \) since \( \tau_k \) is the lowest priority task, this term includes accesses due to all tasks running on processor \( P_i \). In contrast to the derivation of \( S^i_j(t) \), for \( A^i_j(t) \) we can make no assumptions about the synchronisation or otherwise of tasks on processor \( P_j \) with respect to the release of task \( \tau_k \) on processor \( P_i \). The value of \( A^i_j(t) \) is therefore obtained by assuming for each task, that the first job executes as late as possible, i.e. just prior to its worst-case response time, while the next and subsequent jobs execute as early as possible. We assume that the first interfering job of a task \( \tau_k \) has all of its memory accesses as late as possible during its execution, while for subsequent jobs the opposite is true, with execution and memory accesses occurring as early as possible after release of the job. This treatment is similar to the concept of carry-in interference used in the analysis of global multiprocessor fixed-priority scheduling [10], and is illustrated in Figure 2.

Figure 2: Illustration of the carry-in interference analysis.

The number of complete jobs of task \( \tau_k \) contributing accesses in an interval of length \( t \) on processor \( P_j \) is given by:

\[
N^j_k(t) = \left[ \frac{t + R_k - (MD_k + \gamma_{j,k}) \cdot d_{\text{main}}}{T_k} \right]
\]

(24)

Note the term \( (MD_k + \gamma_{j,k}) \cdot d_{\text{main}} \) represents the time for the memory accesses. Hence the total number of accesses possible in an interval of length \( t \) due to task \( \tau_k \) and its related preemption effects is given by:

\[
W^j_k(t) = N^j_k(t) \cdot (MD_k + \gamma_{j,k}) +
\]

\[\min\left(MD_k + \gamma_{j,k}, \left[ \frac{t + R_k - (MD_k + \gamma_{j,k}) \cdot d_{\text{main}} - N^j_k(t) \cdot T_k}{d_{\text{main}}} \right]\right)
\]

(25)

Hence we have:

\[A^i_j(t) = \sum_{k \in \text{lechep}(j)} W^j_k(t)
\]

(26)

The value of \( L^i_j(t) \) is obtained in a similar way to \( A^i_j(t) \), but considering accesses with lower priority than \( j \):

\[L^i_j(t) = \sum_{k \in \text{lechep}(j)} W^j_k(t)
\]

(27)

We note that the carry-in interference has not been accounted for in [24] Equation (5) and (6), resulting in potentially optimistic bounds on the number of competing memory requests in [24].

The number of accesses on the cores are used as input to the bus function (see Section 5), which we use to derive the maximum bus delay that task \( \tau_k \) on processor \( P_i \) can experience during a time interval of length \( t \).

\[I_{\text{BUS}}(i, x, t) = I_{\text{BUS}}(i, x, t) \cdot d_{\text{main}}
\]

(28)

where \( d_{\text{main}} \) is the bus access latency to the global memory.

### 6.4 Global Memory

So far we have assumed a global memory with a constant access latency \( d_{\text{main}} \). Global memory is usually realized based on dynamic random-access memory (DRAM), which needs to be refreshed periodically. Now, we show how to relax the constant-latency assumption to take into account delays imposed by refreshes. We assume a DRAM controller with a First Come First Served (FCFS) scheduling policy so that memory accesses cannot be reordered within the controller. Further, we assume a closed-page policy to minimize the effect of the memory access history on access latencies. We consider two refresh strategies [31]: distributed refresh where the controller refreshes each row at a different time, at regular intervals, and burst refresh where all rows are refreshed immediately one after another.

Under burst refresh, an upper bound on the maximum number of refreshes within an interval of length \( t \) in which \( m \) memory accesses occur is given by:

\[\text{DRAM}_{\text{burst}}(t, m) = \left\lfloor \frac{t}{T_{\text{refresh}}} \right\rfloor \cdot \#\text{rows}
\]

(29)

where \( \#\text{rows} \) is the number of rows in the DRAM module, and \( T_{\text{refresh}} \) is the interval at which each row needs to be refreshed. \( T_{\text{refresh}} \) is usually 64 ms for DDR2 and DDR3 modules.

Under distributed refresh, the upper bound is:

\[\text{DRAM}_{\text{dist}}(t, m) = \min\left(m, \frac{t \cdot \#\text{rows}}{T_{\text{refresh}}} \right)
\]

(30)

This is the case, since at most one memory access can be delayed by each of the refreshes, whereas under burst refresh, a single memory access can be delayed by \( \#\text{rows} \) many refreshes.

As the number of memory accesses within \( t \) is equal to the number of BUS accesses, we can bound the interference due to DRAM refreshes of task \( \tau_k \) on core \( P_i \), as follows:

\[\rho_{\text{DRAM}}(i, x, t) = \text{DRAM}(t, \text{BUS}((i, x, t)) \cdot d_{\text{refresh}}
\]

(31)

where \( d_{\text{refresh}} \) is the refresh latency.
6.5 Multicore Response Time Analysis

The response time $R_i$ of task $τ_i$ is given by the smallest solution to the following recurrence relation:

$$R_i = PD_i + f^{PROC}(i, x, R_i) + f^{BUS}(i, x, R_i) + f^{DRAM}(i, x, R_i)$$

where $f^{PROC}(i, x, R_i)$ is the interference due to processor demand from higher priority tasks running on the same processor assuming no misses on the local memory (see Equation (18)), $f^{BUS}(i, x, R_i)$ is the delay due to bus accesses from tasks running on all cores including MD$_{i}$ (see Equation (28)), and $f^{DRAM}(i, x, R_i)$ is the delay due to DRAM refreshes (see Equation (31)).

Since the response time of each task can depend on the response times of other tasks via the functions (26) and (27) describing memory accesses $A'_j(t)$ and $L'_j(t)$, we use an outer loop around a set of fixed-point iterations to compute the response times of all the tasks, and deal with an apparent circular dependency. Iteration starts with $V_i: R_i = PD_i + MD_i \cdot d_{main}$ and ends when all the response times have converged (i.e. no response time changes w.r.t. the previous iteration), or the response time of a task exceeds its deadline in which case that task is unschedulable. See Algorithm 1 for a pseudo-code algorithm of the response time calculation. Since the response time $R_i$ of a task $τ_i$ is monotonically increasing w.r.t. increases in the response time of any other task, convergence or exceeding a deadline is guaranteed in a bounded number of iterations.

We note that the analysis is sustainable [8] with respect to the processor PD$_{i}$ and memory demands MD$_{i}$ of each task, since values that are smaller than the upper bounds used in the analysis cannot result in a larger response time. This sustainability extends to traces; if any trace of task execution results in practice in a lower processor or memory demand than that considered by the analysis, then this also cannot result in an increase in the response time. Similarly, a decrease in the set of UCBs or ECBs such that they are a subset of those considered by the analysis cannot increase the worst-case response time.

Note that the definitions of MD$_{i}$, PD$_{i}$ and ECB, completely decouple the traces from the response time analysis. This comes at the cost of possible pessimism, but strongly reduces the complexity of the analysis. Different traces may maximize different parameters, meaning that the combination of the parameters in this way may represent a synthetic worst-case that cannot occur in practice.

An alternative solution is to define a multicore response time analysis that is parametric in the execution traces. In the extreme, completely expanding the analysis to explore every combination of traces from different tasks would be intractable. However, as a first step in this direction, response times could be computed for each individual trace of the task of interest $τ_i$, using combined traces for all other tasks. The maximum such response time would then provide an improved upper bound.

6.6 Extensions

Above, we instantiated the Multicore Response Time Analysis (MRTA) framework for relatively simple task and multicore architectural models. In the technical report [2], we briefly discuss extensions including: RTOS and interrupts, dynamic scratchpad management, sharing software resources, open systems and incremental verification, write-back cache policies and multi-level caches. The presented analysis framework is not fine-tuned to specific hardware features or execution scenarios such as burst accesses, since this counteracts its extensibility and generality.

7. EXPERIMENTAL EVALUATION

In this section we describe the results of an experimental evaluation using the MRTA framework 2. For the evaluation, we use the Mälardalen benchmark suite [18] to provide traces. We model a multicore system based on an ARM Cortex A5 multicore 3 as a reference architecture to provide a cache configuration and memory and bus latencies. As this work is intended to provide an overview of our generic and extensible framework, we do not model all details of the specific multicore architecture. A case study comparing measurements on a real hardware with the computed bounds is future work.

![Multicore Architecture Case Study: m = 4 cores with local caches connected via a common bus to a global memory.](http://www.arm.com/products/processors/cortex-a/cortex-a5.php)
policy. All other parameters remain the same as in the reference architecture. The performance on the isolation architecture corresponds to the traditional two-step approach to timing verification with context-independent WCETs. The second alternative, referred to as uncached architecture, assumes no local caches except for a buffer of size 1, and uses Round-Robin bus arbitration. All other parameters are again the same as the reference configuration.

The traces for the benchmarks were generated using the gem5 instruction set simulator [13] and contain statically linked library calls. As the benchmark code corresponds to independent tasks, no data is shared between the tasks. Table 1 shows information for a representative selection of the 39 benchmark programs used to provide traces including the total number of instructions (which is equal to the processor demand), the number of read/write operations, the memory demand, and the maximum number of UCBs and ECBs on the reference multicore architecture. Complete information for all benchmarks can be found in Table 1 of the technical report [2]. Each benchmark is assigned only one trace, which is sufficient due to the simple structure of the benchmark suite: The benchmarks are either single-path or worst-case input is provided. Despite the rather simple structure of the benchmarks, the tasks show a strong variation in processor and memory demand. As all benchmarks exhibit only one trace, the worst-case processor and memory demand coincide. Evaluation of more complex tasks including evaluation of the trade-off between pessimism of independent upper bounds and the computational complexity of explicit traces remains as future work.

We identify three main sources of over-approximation of our multicore response time analysis framework: The number of memory accesses on the same core cannot be precisely estimated due to imprecision in the pre-emption cost analysis. The interference due to bus accesses may be pessimistic as not all tasks running on another core can simultaneously access the bus. The DRAM refreshes are assumed too frequently if the number of main memory accesses is over-approximated. A sophisticated evaluation of the precision of our analysis requires measurements on a real architecture, which we cannot yet provide. However, the different architecture configurations provide an estimate of the influence of the different sources of pessimism. The reference architecture with a perfect bus eliminates any pessimism due to bus interference and DRAM accesses. Only the pessimism of the pre-emption cost analysis remains, which has been quantified in [3]. The full-isolation architecture removes all pessimism due to the bus interference and the pre-emption costs, and thus only suffers from the pessimism in the DRAM analysis.

We evaluated the guaranteed performance of the various configurations as computed using the MRTA framework on a large number of randomly generated task sets. The task set parameters were as follows:

- The default task set size was 32, with 8 tasks per core.
- Each task was randomly assigned a trace from Table 1.
- The base WCET per task $T_r$, needed solely to set the task periods and deadline, was defined as:
  \[
  C_i = PD_i + MD_i \cdot d_{main} + DRAM(PD_i + MD_i \cdot d_{main}, MD_i) \cdot d_{fetch}
  \]
  $C_i$ denotes the execution time of the task without any interference from any other task.
- The task utilizations were generated using UUnifast [12] with an equal utilization assumed for each core.
- Task periods were set based on task utilization and base WCET, i.e., $T_i = C_i/U_i$.
- Task deadlines were implicit.
- Priorities were assigned in deadline monotonic order.

We note that the processor utilization is often not the limiting factor on a multicore system, but the memory utilization, defined as:

\[
U_{BUS} = \sum_i MD_i / T_i
\]

Only if $U_{BUS} \leq 1$, can the tasks be scheduled.

The utilization per core was varied from 0.025 to 0.975 in steps of 0.025. For each utilization value, 1000 tasksets were generated and the schedulability was determined for each architectural configuration. Figure 4 shows the number of schedulable task sets plotted against the core utilization (computed using the base WCETs) and Figure 5 against the bus utilization $U_{BUS}$. The full-isolation architecture (light blue) results in a high number of bus accesses even at low core utilizations, followed by Round-Robin (dark blue line) and then TDMA (pink line). The full-isolation architecture removes all pessimism due to the bus interference and the pre-emption costs, and thus only suffers from the pessimism in the DRAM analysis.

Most traces from Table 1 have a high memory demand, which results in a high number of bus accesses even at low core utilizations. Consequently, most task sets are not schedulable even with a perfect bus. The fixed-priority bus (green line) where the memory accesses inherit the task priority shows the best performance, followed by Round-Robin (dark blue line) and then TDMA (pink line). The full-isolation architecture (light blue) implementing TDMA and cache partitioning on the local caches performs nearly as well as the TDMA architecture, which indicates that the increased execution times due to cache partitioning only have a minor impact in this case. Note for TDMA and Round-Robin, we assume a cycle with 2 slots per processor. The FIFO bus shows the lowest performance, similar to that of an uncached architecture, which uses Round-Robin. The worst-case arrival pattern for a FIFO bus (black line) assumes that each potentially co-running task has issued bus requests just
use the weighted schedulability measure [9], to show how schedulability varies with these parameters.

As the memory demand of the benchmark traces is high, the bus latency $d_{main}$ has a tremendous impact on overall schedulability (see Figure 6). The bus latency affects all bus policies similarly.

By increasing the number of cores, the number of tasks also increases (assuming a fixed number of tasks per core) and so does the bus utilization. The performance of all configurations decreases (see Figure 7) as fewer task sets are deemed schedulable, irrespective of the bus policy.

As might be expected, longer DRAM refresh latencies have a significant detrimental effect on schedulability for all configurations, see Figure 8.

8. CONCLUSIONS

In this paper, we introduced a Multicore Response Time Analysis (MRTA) framework. This framework is extensible to different multicore architectures, with various types and arrangements of local memory, and different arbitration policies for the common interconnects. In this initial paper, we instantiated the MRTA framework assuming single level local data and instruction memories (cache or scratchpads), and for a variety of memory bus arbitration policies, including: Round-Robin, FIFO, Fixed-Priority, Processor-Priority, and TDMA.

The MRTA framework provides a general approach to timing verification for multicore systems that is parametric in the hardware configuration (common interconnect, local memories, number of cores etc.) and so can be used both at the architectural design stage to compare the guaranteed levels of performance obtained with different hardware configurations, and also during development to verify the timing behaviour of a specific system.

The MRTA framework decouples response time analysis from a reliance on context independent WCET values. Instead, the analysis formulates response times directly from the demands on the bus and core utilization. By increasing the number of cores, the number of tasks also increases (assuming a fixed number of tasks per core) and so does the bus utilization. The performance of all configurations decreases (see Figure 7) as fewer task sets are deemed schedulable, irrespective of the bus policy.

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and semi-partitioned scheduling policies. We also plan to run detailed (cycle accurate) simulations of the multicore architectures to examine the effectiveness of the MRTA framework compared to observed behaviour.

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