Response Time Analysis of Synchronous Data Flow Programs on a Many-Core Processor

Hamza Rihani, Matthieu Moy, Claire Maiza, Robert I. Davis, Sebastian Altmeyer

RTNS'16, October 19, 2016

RTNS * Artifact Evaluated *

Consistent * Complete * Well documented * Easy to reuse *

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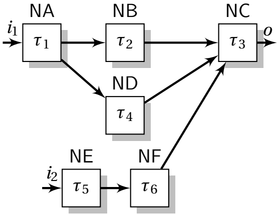
Execution of Synchronous Data Flow Programs



High level representation

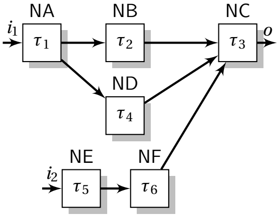
Single-core

code generation

```
int main_app(i1, i2)
{
     na = NA(i1);
     ne = NE(i2);
     nb = NB(na);
     nd = ND(na);
     nf = NF(ne);
     o = NC(nb,nd,nf);
     return o;
}
```

static non-preemptive scheduling

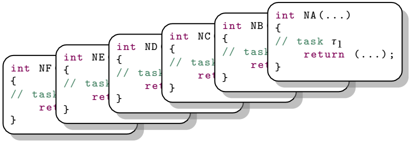
Execution of Synchronous Data Flow Programs



High level representation

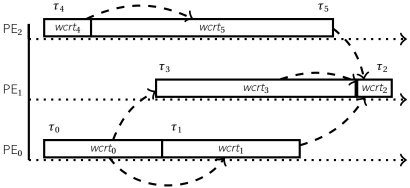
Multi/Many-core

code generation



```
int NA(...)
{
// task τ1
    return (...);
}
```

static non-preemptive scheduling



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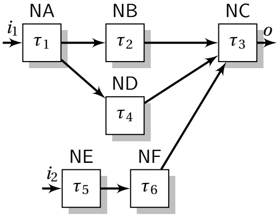

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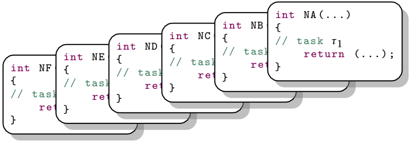

```
int NA(...)
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// task τ1
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}
```
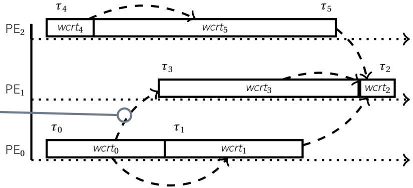
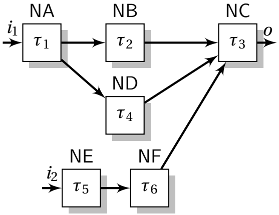

int NF
int NE
int ND
int NC
int NB

static non-preemptive scheduling



✓ Respect the dependency constraints

Execution of Synchronous Data Flow Programs



High level representation

Multi/Many-core

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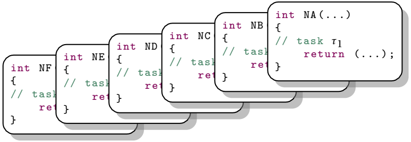

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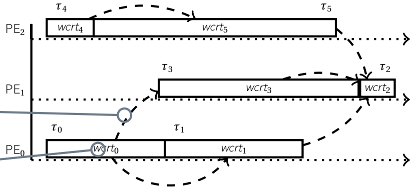
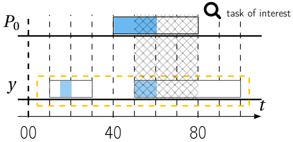


✓ Respect the dependency constraints

✓ Set the release dates to get precise upper bounds on the interference

Contributions

1. Precise accounting for interference on shared resources in a many-core processor



Contributions

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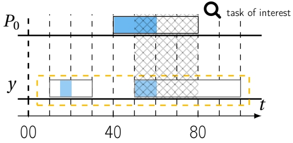
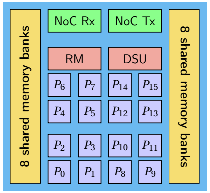


2. Model of a multi-level arbiter to the shared memory



Contributions

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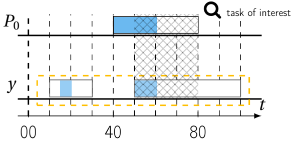

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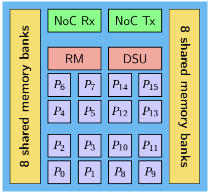

3. Response time and release dates analysis respecting dependencies.

Outline

1. Motivation and Context
2. Models Definition
   - Architecture Model
   - Execution Model
   - Application Model
3. Multicore Response Time Analysis of SDF Programs
4. Evaluation
5. Conclusion and Future Work

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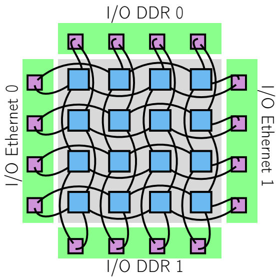
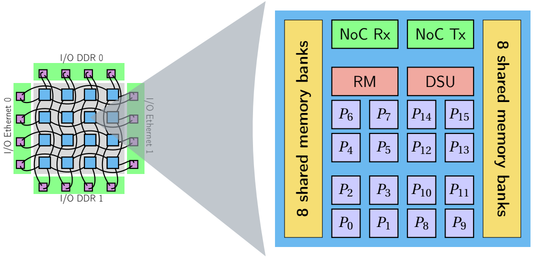
Architecture Model



- Kalray MPPA 256 Bostan
- 16 compute clusters + 4 I/O clusters
- Dual NoC

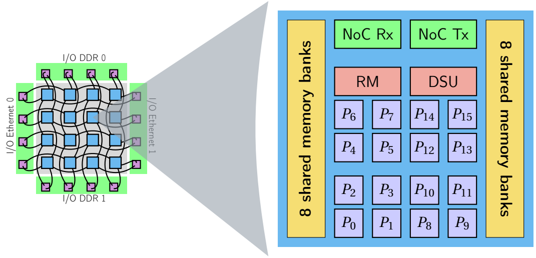
Architecture Model



Per cluster:

- 16 cores + 1 Resource Manager
- NoC Tx, NoC Rx, Debug Unit
- 16 shared memory banks per cluster (total 2 MB)

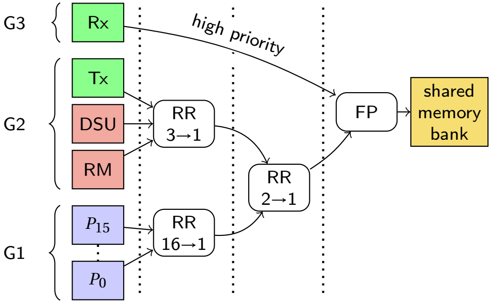
Architecture Model



I/O DDR 0
I/O DDR 1
I/O Ethernet 0
I/O Ethernet 1
8 shared memory banks
NoC Rx
NoC Tx
RM
DSU
P_6 P_7 P_{14} P_{15}
P_4 P_5 P_{12} P_{13}
P_2 P_3 P_{10} P_{11}
P_0 P_1 P_8 P_9
8 shared memory banks

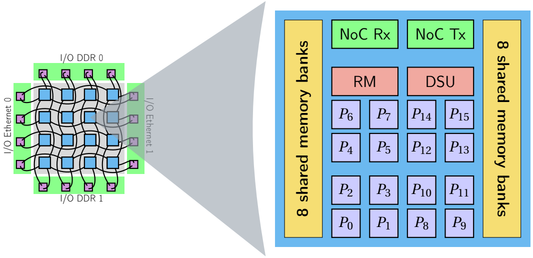
Per cluster:

- 16 cores + 1 Resource Manager
- NoC Tx, NoC Rx, Debug Unit
- 16 shared memory banks per cluster (total 2 MB)
- Multi-level bus arbiter per memory bank



G3
Rx
high priority
G2
Tx
DSU
RM
RR 3→1
RR 2→1
FP
shared memory bank
G1
P_{15}
P_0
RR 16→1

Architecture Model



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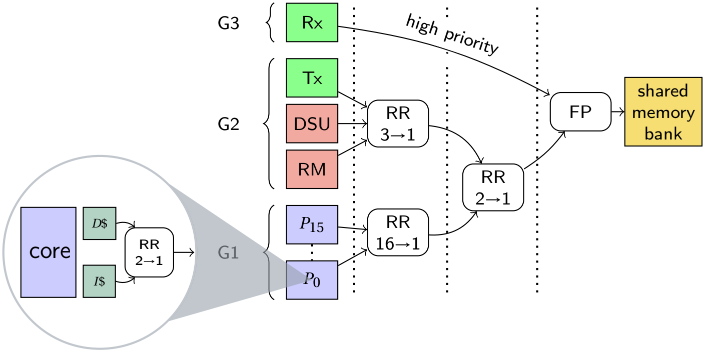
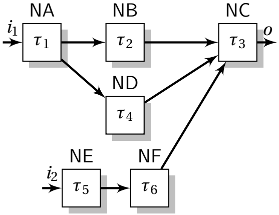
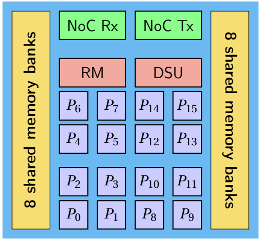


Execution Model





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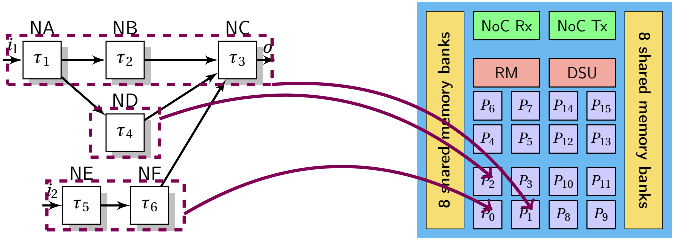
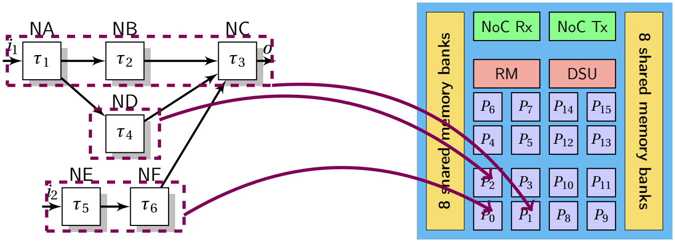
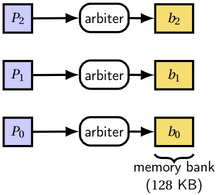


- Tasks mapping on cores
- Static non-preemptive scheduling

Execution Model





- Tasks mapping on cores
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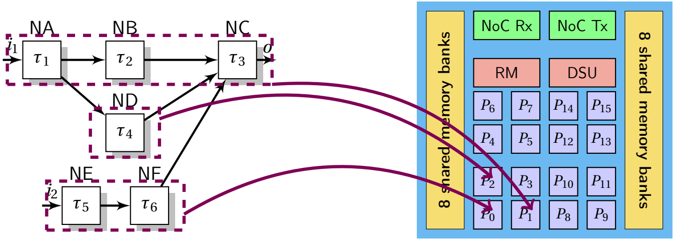
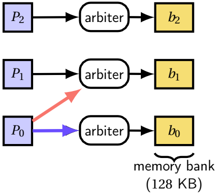
- Spatial Isolation

  different tasks go to different memory banks

Execution Model





- Tasks mapping on cores
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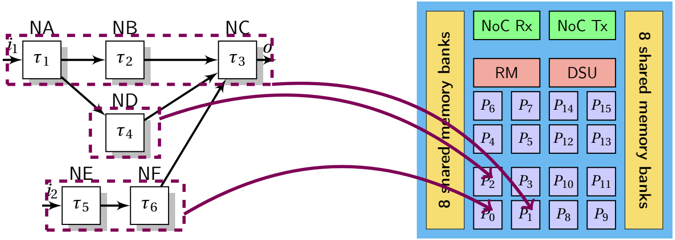
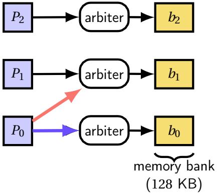
- Interference from communications

Execution Model





- Tasks mapping on cores
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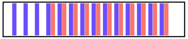
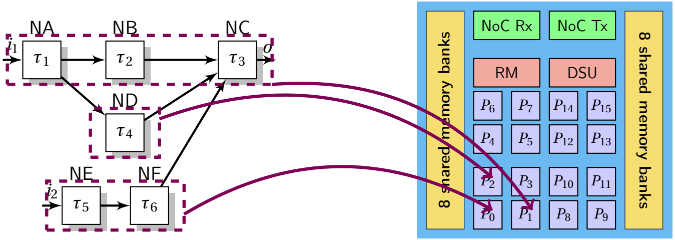
  different tasks go to different memory banks
- Interference from communications
- Execution model:
  - execute in a "local" bank
  - write to a "remote" bank

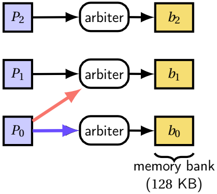
Single phase: execute *and* write data.

memory access pattern



Execution Model





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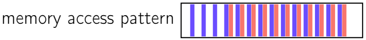
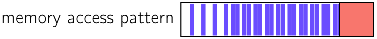
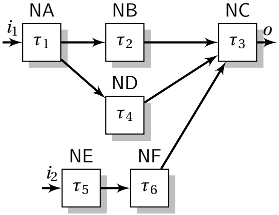


Two phases: execute *then* write data.

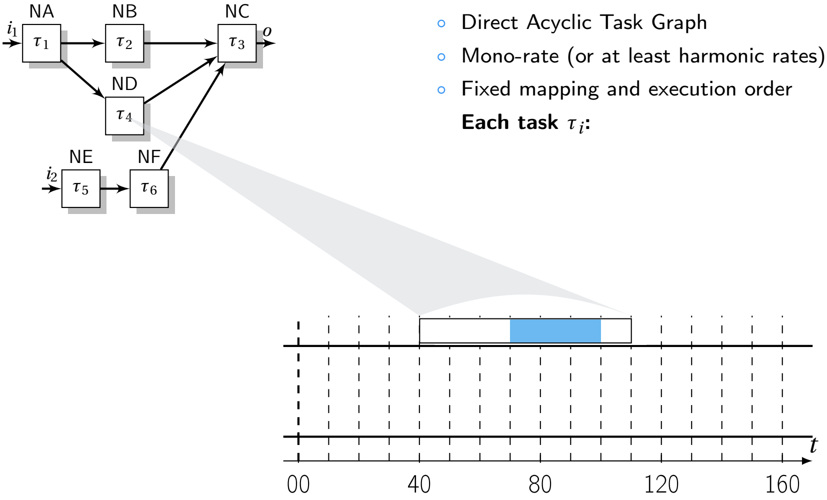


Application Model



- Direct Acyclic Task Graph
- Mono-rate (or at least harmonic rates)
- Fixed mapping and execution order

Application Model



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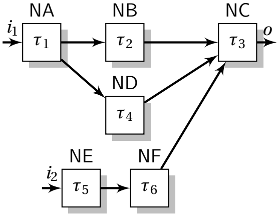
Each task τ_i:

Application Model



- Direct Acyclic Task Graph
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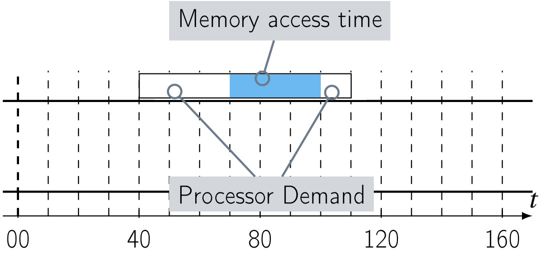
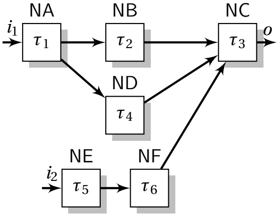
Each task τ_i:

- Processor Demand, Memory Demand


Memory access time

Processor Demand

Application Model



- Direct Acyclic Task Graph
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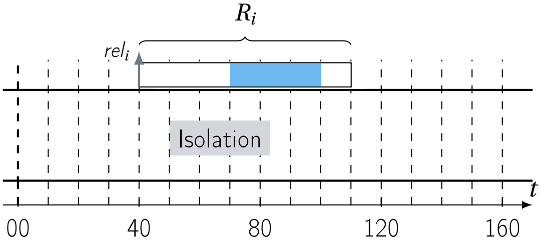
Each task τ_i:

- Processor Demand, Memory Demand
- Release date (rel_i), response time (R_i)



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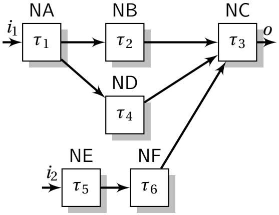

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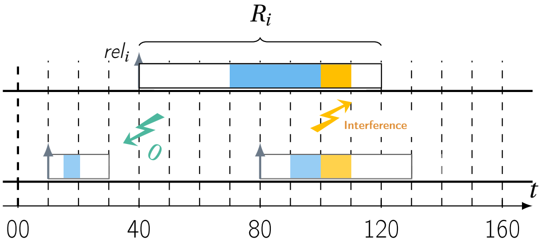
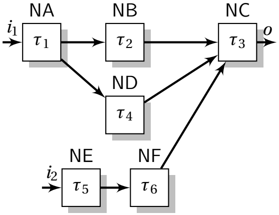


Application Model



- Direct Acyclic Task Graph
- Mono-rate (or at least harmonic rates)
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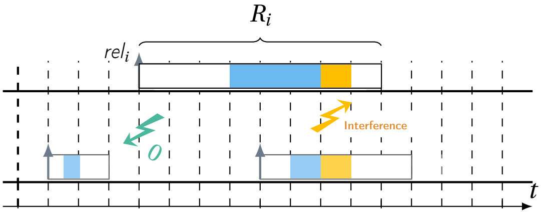
Each task τ_i:

- Processor Demand, Memory Demand
- Release date (*rel*$_i$), response time (R_i)



Find R_i (including the interference)

Find *rel*$_i$ respecting precedence constraints

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Response Time Analysis

$$R = PD + I^{BUS}(R)$$

- Response Time

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- Response Time
  - Processor Demand

Response Time Analysis

$$R = PD + I^{BUS}(R)$$

- Response Time
  - Processor Demand
    - Bus Interference

(given a model of the bus arbiter)

Response Time Analysis

$$R = PD + I^{BUS}(R) + I^{PROC}(R) + I^{DRAM}(R)$$

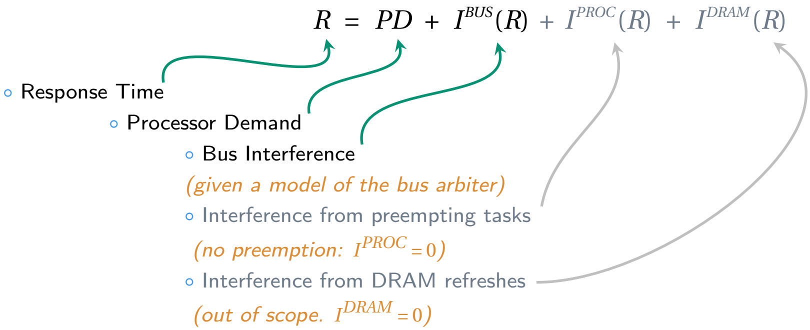
- Response Time
  - Processor Demand
    - Bus Interference

      (given a model of the bus arbiter)
    - Interference from preempting tasks

      (no preemption: $I^{PROC} = 0$)
    - Interference from DRAM refreshes

      (out of scope. $I^{DRAM} = 0$)

Response Time Analysis



$$R = PD + I^{BUS}(R) + I^{PROC}(R) + I^{DRAM}(R)$$

- Response Time
- Processor Demand
- Bus Interference

(given a model of the bus arbiter)

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- Recursive formula ⇒ fixed-point algorithm.

Response Time Analysis

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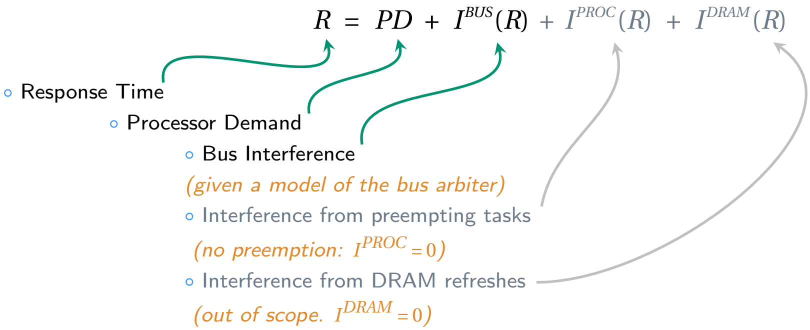
- Multiple shared resources (memory banks)

Response Time Analysis



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- Recursive formula ⇒ fixed-point algorithm.
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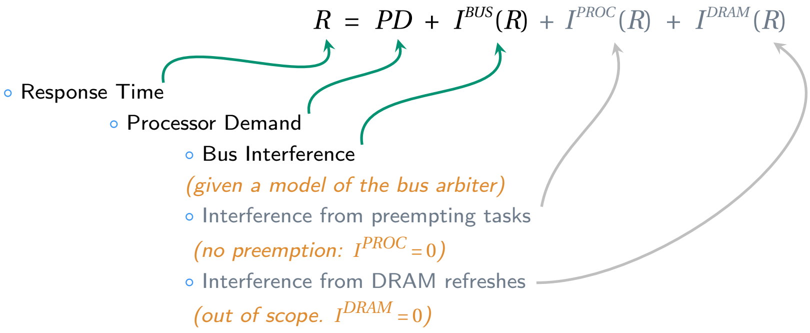
$$I^{BUS}(R) = \sum_{b \in B} I_b^{BUS}(R)$$

where B: a set of memory banks

Response Time Analysis



$$R = PD + I^{BUS}(R) + I^{PROC}(R) + I^{DRAM}(R)$$

- Response Time
- Processor Demand
- Bus Interference

(given a model of the bus arbiter)

- Interference from preempting tasks

(no preemption: $I^{PROC} = 0$)

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(out of scope. $I^{DRAM} = 0$)

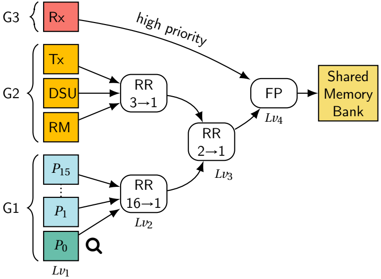
- Recursive formula ⇒ fixed-point algorithm.
- Multiple shared resources (memory banks)

$$I^{BUS}(R) = \sum_{b \in B} I_b^{BUS}(R)$$

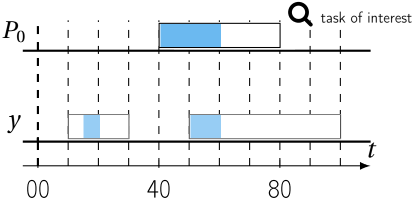
where B: a set of memory banks

Requires a model of the bus arbiter

Model of the MPPA Bus



I_b^{BUS}: delay from all accesses + concurrent ones



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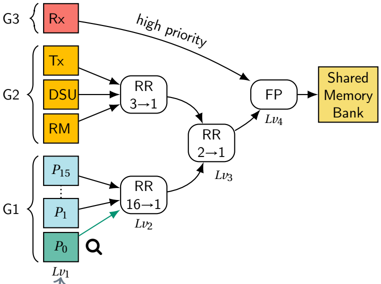
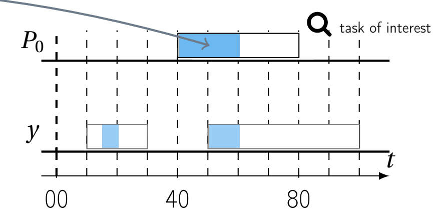


I_b^{BUS}: delay from all accesses + concurrent ones

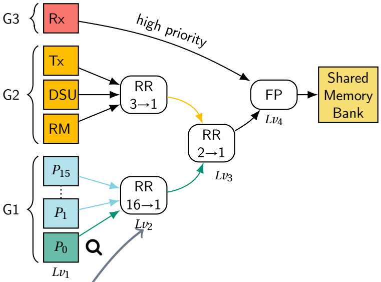
S_i^b: number of accesses of task τ_i to bank b

S_i^b = Memory Demand to bank b

$Lv_1 = S_i^b$



Model of the MPPA Bus



I_b^{BUS}: delay from all accesses + concurrent ones

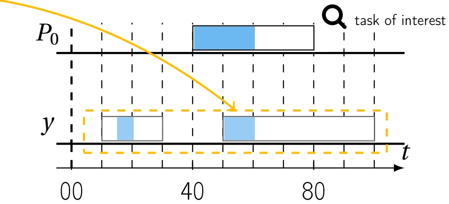
S_i^b: number of accesses of task τ_i to bank b

S_i^b = Memory Demand to bank b

$A_i^{y,b}$: number of concurrent accesses from core y to bank b

$$Lv_1 = S_i^b$$

$$Lv_2 = Lv_1 + \sum_{y=1}^{15} \min(A_i^{y,b}, Lv_1)$$



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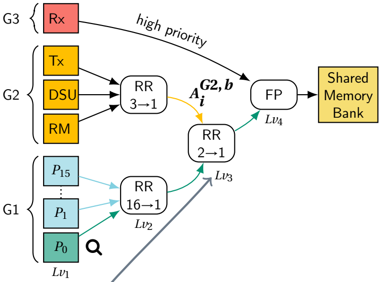

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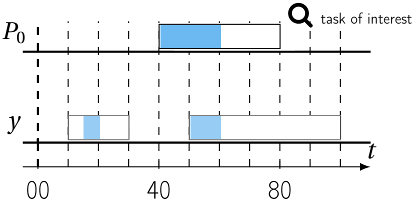
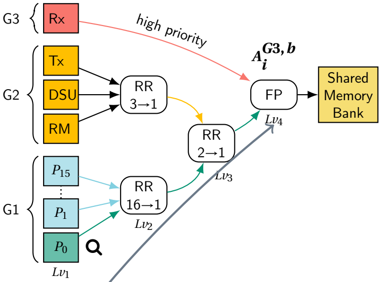


Model of the MPPA Bus



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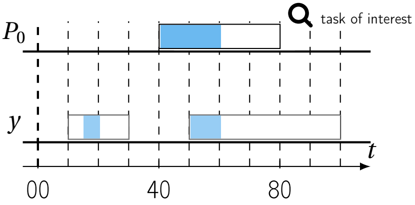
$$Lv_4 = Lv_4 + A_i^{G3,b}$$



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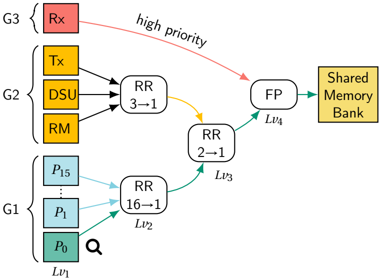

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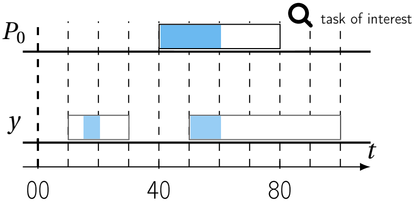
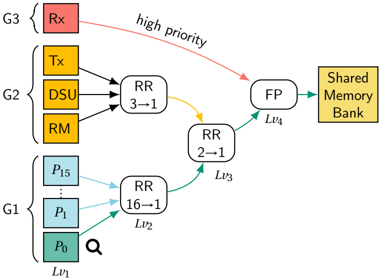


$$I_b^{BUS} = Lv_4 \times \text{Bus Delay}$$

Model of the MPPA Bus



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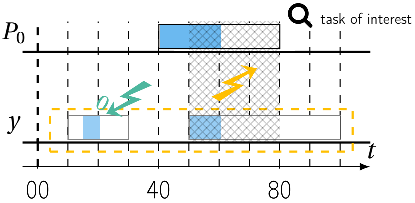
$A_i^{y,b} = \sum$ overlapping concurrent accesses

$$
\begin{aligned}
Lv_1 &= S_i^b \\
Lv_2 &= Lv_1 + \sum_{y=1}^{15} \min(A_i^{y,b}, Lv_1) \\
Lv_3 &= Lv_2 + \min(A_i^{G2,b}, Lv_2) \\
Lv_4 &= Lv_4 + A_i^{G3,b}
\end{aligned}
$$



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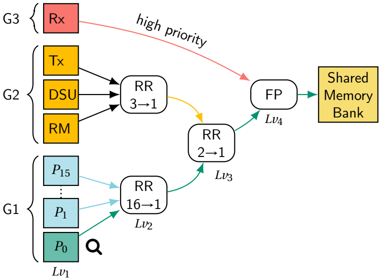
Model of the MPPA Bus



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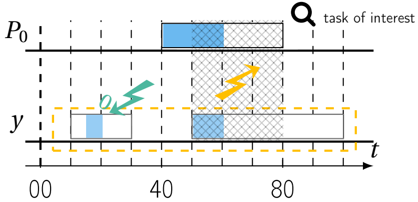
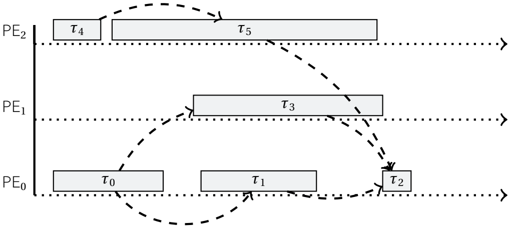


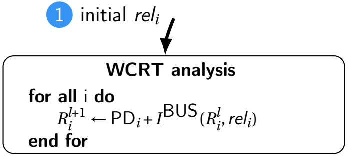
$I_b^{BUS} = Lv_4 \times$ Bus Delay

⚠ $A_i^{y,b}$ depends on rel_i and R_i

Response Time Analysis with Dependencies



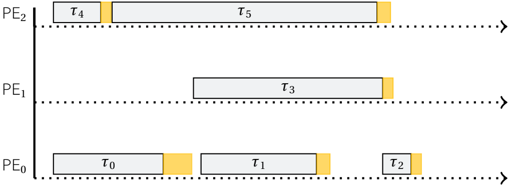
1 Start with initial release dates.

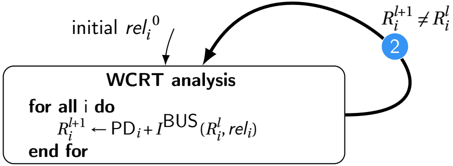


WCRT analysis

```
for all i do
    $R_i^{l+1} \leftarrow \mathrm{PD}_i + I^{\mathrm{BUS}}(R_i^l, rel_i)$
end for
```

Response Time Analysis with Dependencies





WCRT analysis

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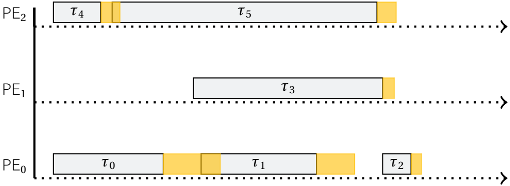
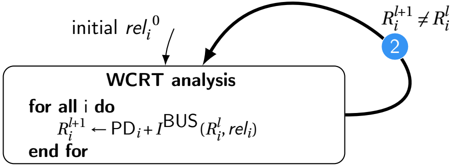
end for
```

1. Start with initial release dates.
2. Compute response times

   …

Response Time Analysis with Dependencies





WCRT analysis

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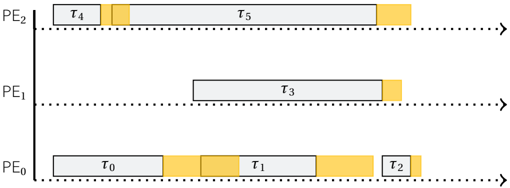
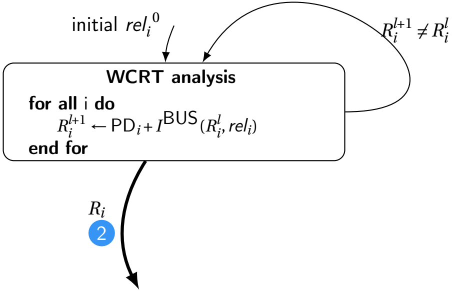
   … …

Response Time Analysis with Dependencies



1. Start with initial release dates.
2. Compute response times

   … … … a fixed-point is reached!



WCRT analysis

```
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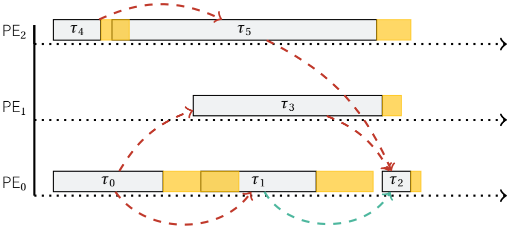
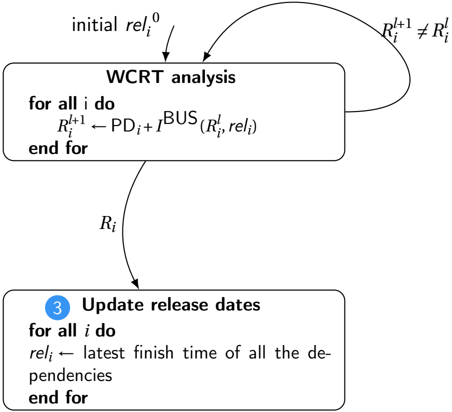
    $R_i^{l+1} \leftarrow \mathrm{PD}_i + I^{\mathrm{BUS}}(R_i^l, rel_i)$
end for
```

Response Time Analysis with Dependencies



1. Start with initial release dates.
2. Compute response times

   … … … a fixed-point is reached!
3. Update the release dates.



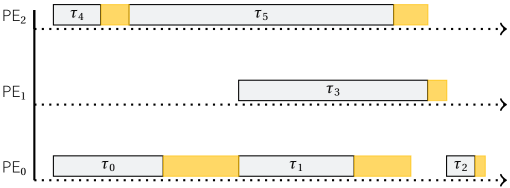
WCRT analysis

```
for all i do
    $R_i^{l+1} \leftarrow \mathrm{PD}_i + I^{\mathrm{BUS}}(R_i^l, rel_i)$
end for
```

3 **Update release dates**

```
for all $i$ do
$rel_i \leftarrow$ latest finish time of all the dependencies
end for
```

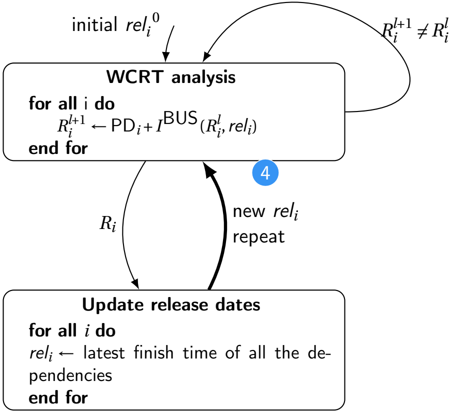
Response Time Analysis with Dependencies



1. Start with initial release dates.
2. Compute response times

   ... ... a fixed-point is reached!
3. Update the release dates.
4. Repeat until no release date changes

   (another fixed-point iteration).



WCRT analysis

```
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```

Update release dates

```
for all $i$ do
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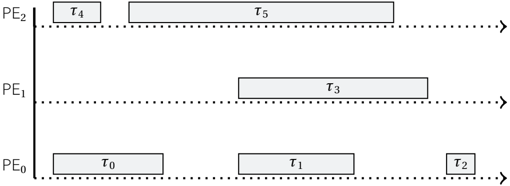
end for
```

Response Time Analysis with Dependencies



1. Start with initial release dates.
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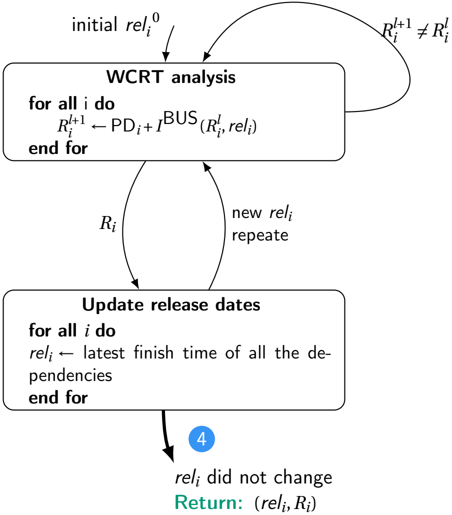

WCRT analysis

```
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end for
```

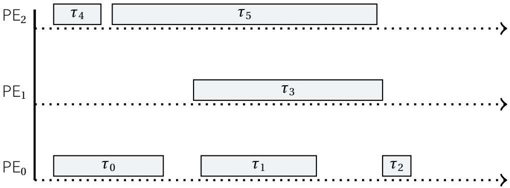
Update release dates

```
for all $i$ do
$rel_i \leftarrow$ latest finish time of all the dependencies
end for
```

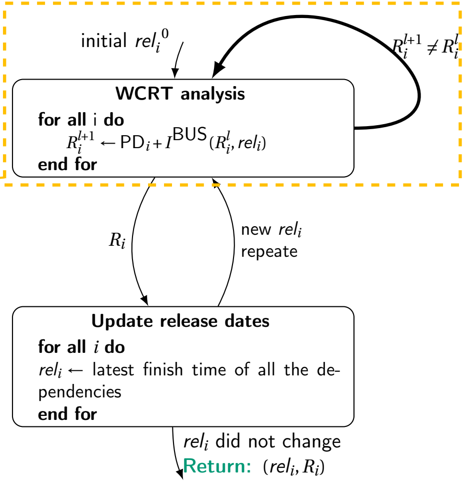
rel_i did not change

Return: (rel_i, R_i)

Convergence Toward a Fixed-point



- Convergence of the 1^{st} fixed-point iteration:



initial rel_i^0

$R_i^{l+1} \neq R_i^l$

WCRT analysis

```
for all i do
    $R_i^{l+1} \leftarrow \text{PD}_i + I^{\text{BUS}}(R_i^l, rel_i)$
end for
```

R_i

new rel_i repeate

Update release dates

```
for all $i$ do
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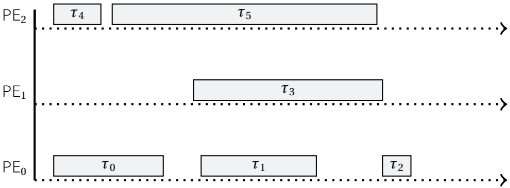
end for
```

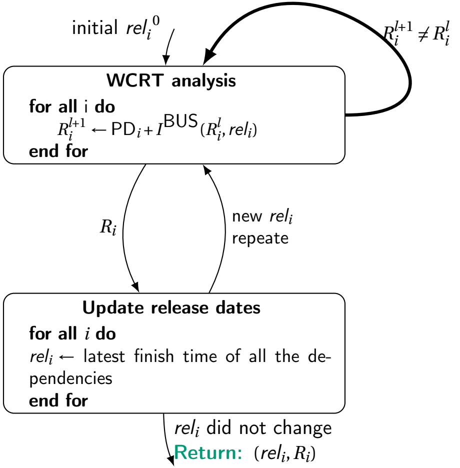
rel_i did not change

Return: (rel_i, R_i)

Convergence Toward a Fixed-point



- Convergence of the 1^{st} fixed-point iteration:
  - Monotonic and bounded ✓



WCRT analysis

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```

Update release dates

```
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end for
```
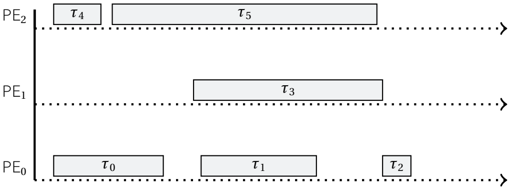

Return: (rel_i, R_i)

Convergence Toward a Fixed-point



- Convergence of the 1^{st} fixed-point iteration:
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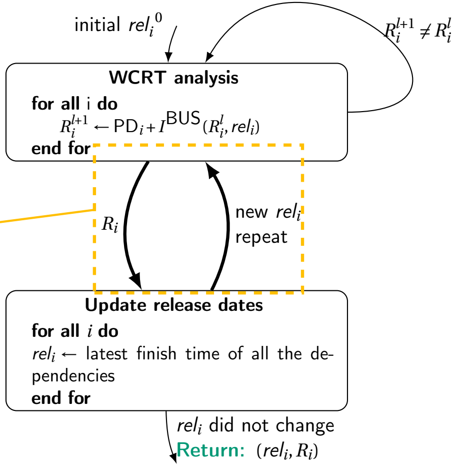
- Convergence of the 2^{nd} fixed-point iteration:



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```

R_i

new rel_i
repeat

Update release dates

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for all $i$ do
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end for
```
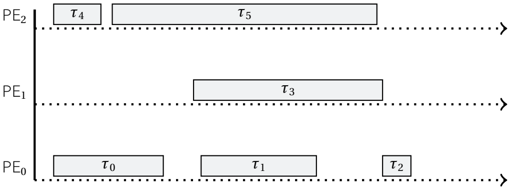
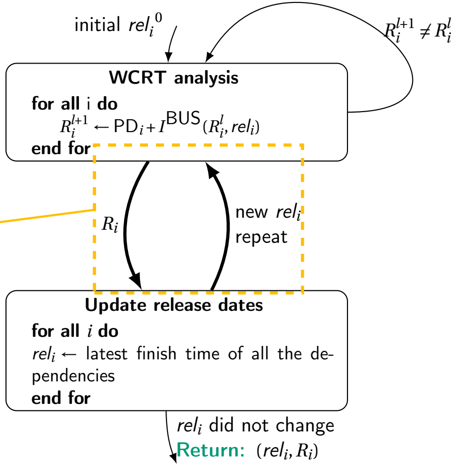

rel_i did not change

Return: (rel_i, R_i)

Convergence Toward a Fixed-point



- Convergence of the 1^{st} fixed-point iteration:
    - Monotonic and bounded ✓
- Convergence of the 2^{nd} fixed-point iteration:
    - no monotonicity: R_i and rel_i may grow or shrink at each iteration. ?



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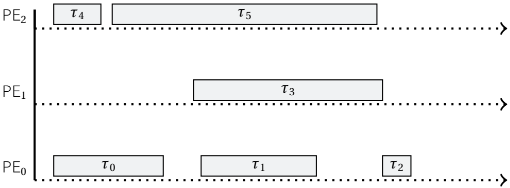
Convergence Toward a Fixed-point



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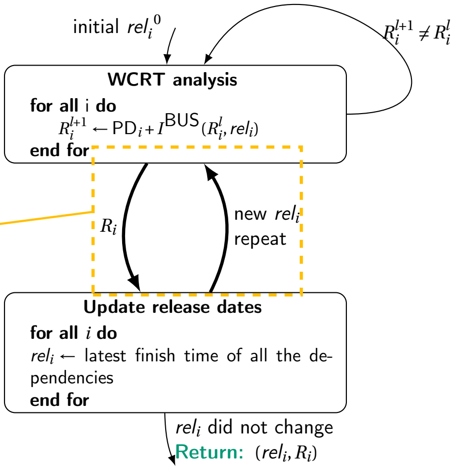
Theorem

At each iteration, <u>at least one task</u> finds its final release date.

Full proof in our technical report:
http://www-verimag.imag.fr/TR/TR-2016-1.pdf



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Update release dates

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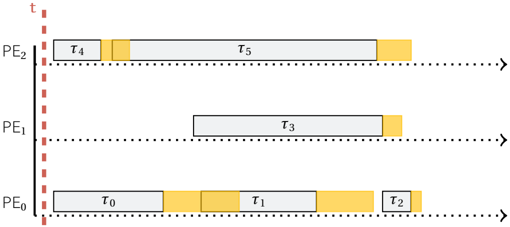

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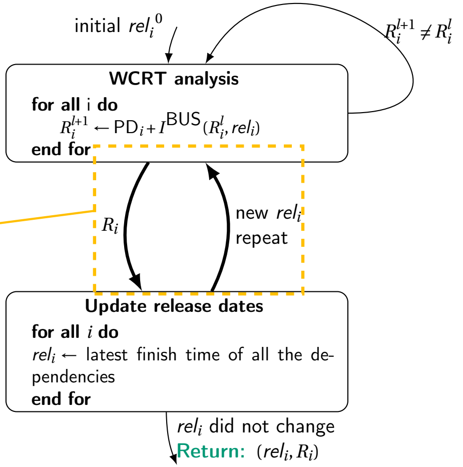

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WCRT analysis

```
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```

R_i

new rel_i repeat

Update release dates

```
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```

rel_i did not change

Return: (rel_i, R_i)

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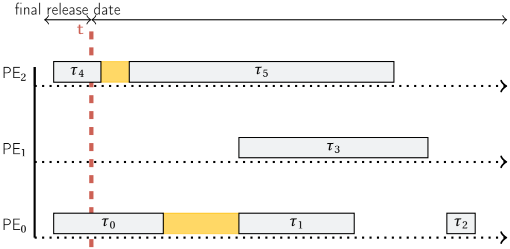
Convergence Toward a Fixed-point



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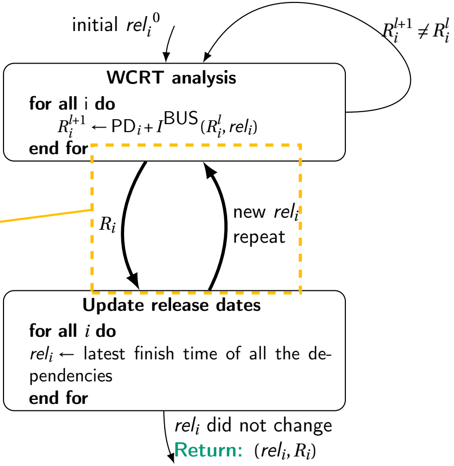

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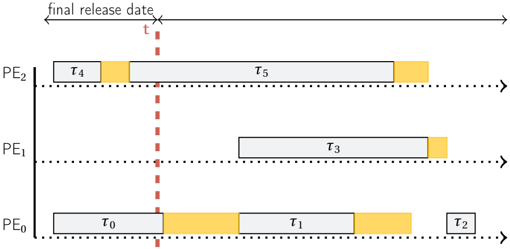
Convergence Toward a Fixed-point



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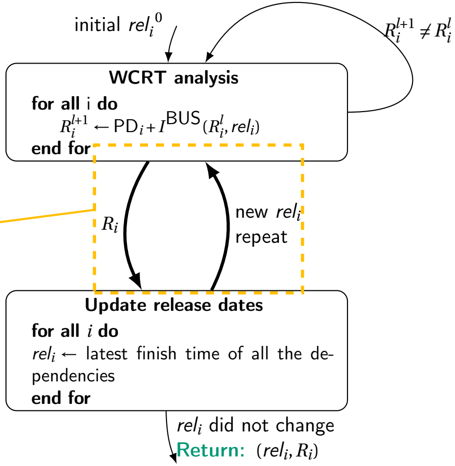

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for all $i$ do
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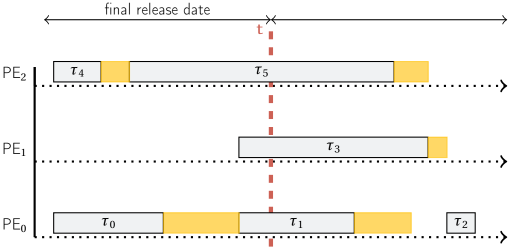
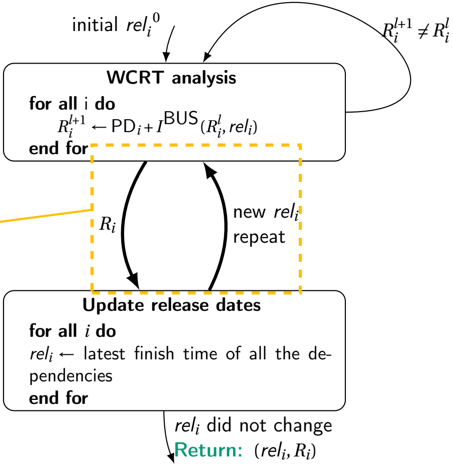
end for
```

Return: (rel_i, R_i)

Convergence Toward a Fixed-point



- Convergence of the 1^{st} fixed-point iteration:
  - Monotonic and bounded ✓
- Convergence of the 2^{nd} fixed-point iteration:
  - no monotonicity: R_i and rel_i may grow or shrink at each iteration. ?



WCRT analysis

```
for all i do
    $R_i^{l+1} \leftarrow \mathrm{PD}_i + I^{\mathrm{BUS}}(R_i^l, rel_i)$
end for
```

Update release dates

```
for all $i$ do
    $rel_i \leftarrow$ latest finish time of all the dependencies
end for
```

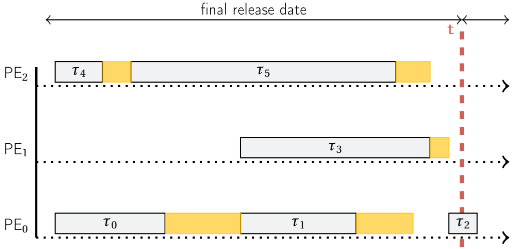
Return: (rel_i, R_i)

Theorem

At each iteration, at least one task finds its final release date.

Full proof in our technical report:
http://www-verimag.imag.fr/TR/TR-2016-1.pdf

Convergence Toward a Fixed-point



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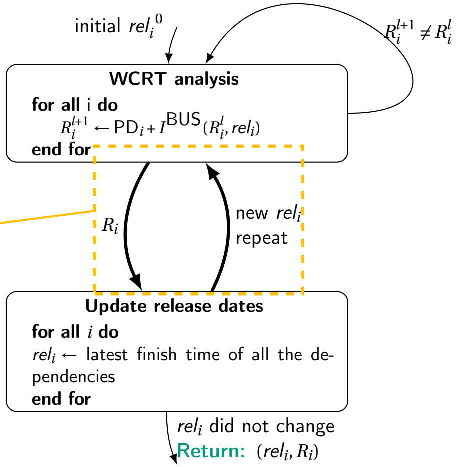

initial rel_i^0

$R_i^{l+1} \neq R_i^l$

WCRT analysis

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end for
```

R_i

new rel_i
repeat

Update release dates

```
for all i do
rel_i ← latest finish time of all the dependencies
end for
```

rel_i did not change

Return: (rel_i, R_i)

Outline

1 Motivation and Context

2 Models Definition
- Architecture Model
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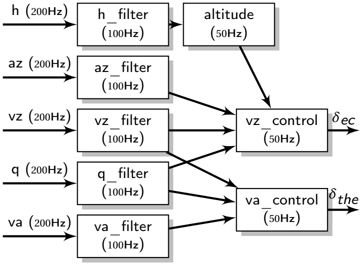
3 Multicore Response Time Analysis of SDF Programs

4 Evaluation

5 Conclusion and Future Work

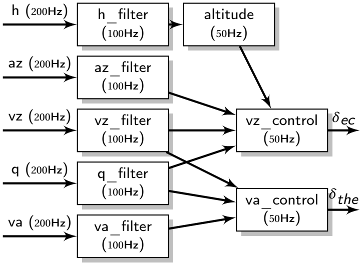
Evaluation: ROSACE Case Study [1]



- Flight management system controller

[1] Pagetti et al., RTAS 2014

Evaluation: ROSACE Case Study [1]



- Flight management system controller
- Receive from sensors and transmit to actuators

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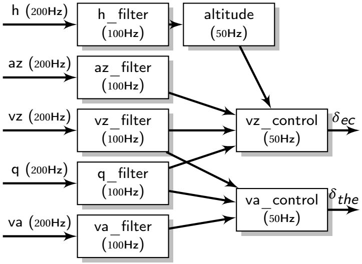
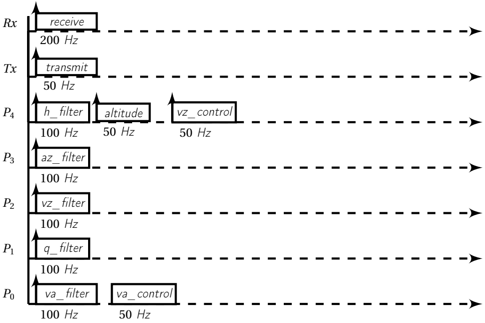


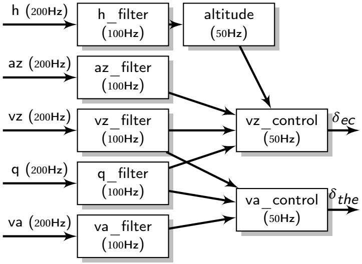


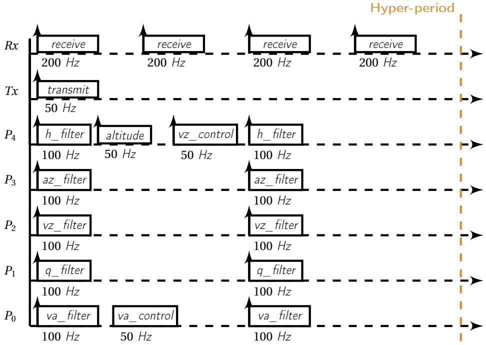
- Flight management system controller
- Receive from sensors and transmit to actuators
- **Assumptions:**

  Tasks are mapped on 5 cores
  Debug Support Unit is disabled
  Context switches are over-approximated constants

[1] Pagetti et al., RTAS 2014

Evaluation: ROSACE Case Study [1]





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Evaluation: ROSACE Case Study

Task	Processor Demand (cycles)	Memory Demand (accesses)
altitude	275	22
az_filter	274	22
h_filter	326	24
va_control	303	24
va_filter	301	23
vz_control	320	25
vz_filter	334	25

Table: Task profiles of the FMS controller

- Profile obtained from measurements

Evaluation: ROSACE Case Study

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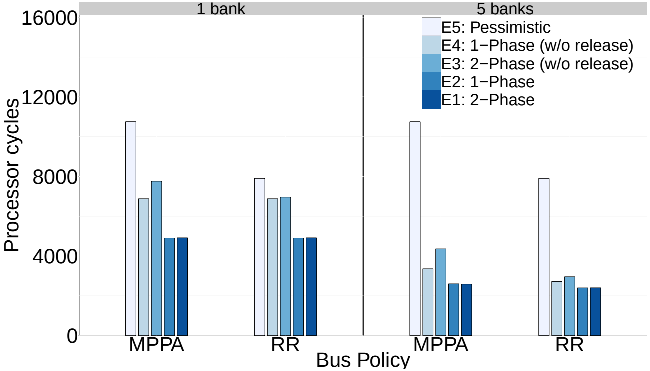
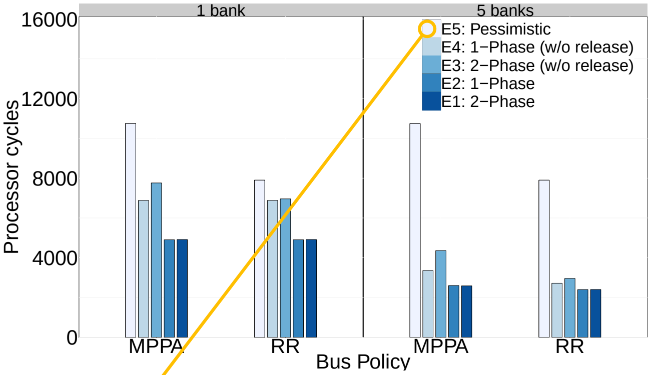
⚗ Experiments: Find the smallest schedulable hyper-period

Evaluation: Experiments



Smallest schedulable hyper-period

Evaluation: Experiments

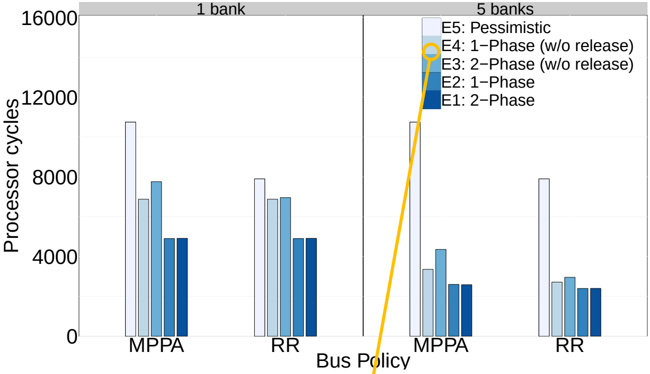


Smallest schedulable hyper-period

E5: All accesses interfere

- Pessimistic assumption: High priority tasks are bounded by 1 access per bank

Evaluation: Experiments



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- Pessimistic assumption: High priority tasks are bounded by 1 access per bank

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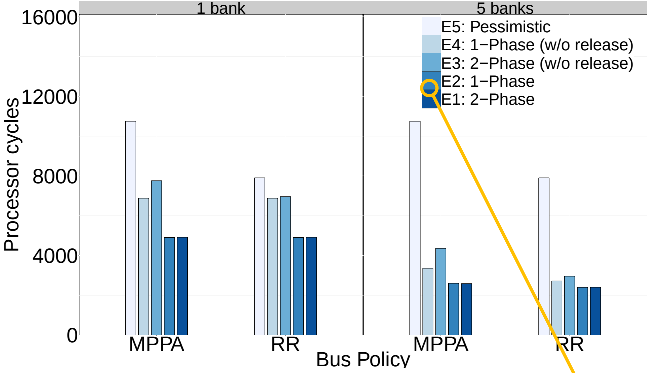
E4, E3: We don't use the release dates

Evaluation: Experiments



Smallest schedulable hyper-period

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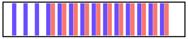
E2, E1: Our approach. We use the release dates

Evaluation: Experiments

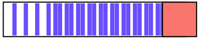
1-Phase model

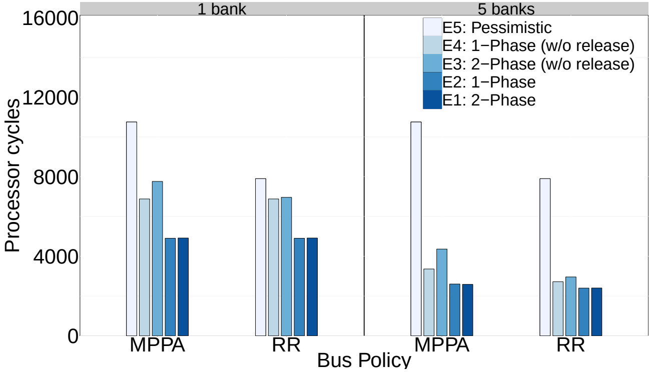
memory access pattern



2-Phase model

memory access pattern





Smallest schedulable hyper-period

- Pessimistic assumption: High priority tasks are bounded by 1 access per bank
- Phases are modeled as sub-tasks

E5: All accesses interfere

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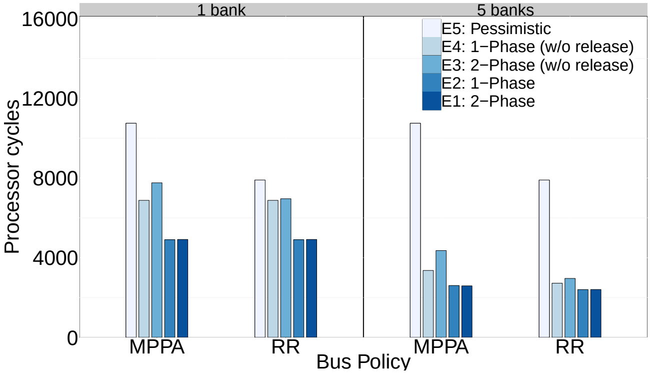
Evaluation: Experiments

Taking into account the memory banks improves the analysis with a factor in $[1.77, 2.52]$



Smallest schedulable hyper-period

RTNS * Artifact * Evaluated * Consistent * Complete * Well documented * Easy to reuse *

	E5/E1	E5/E2	E3/E1	E4/E2	E2/E1	E4/E3
MPPA	4.15	4.12	1.68	1.29	~1.01	0.77
RR	3.3	3.29	1.24	1.13	~1.01	0.91

Speedup factors

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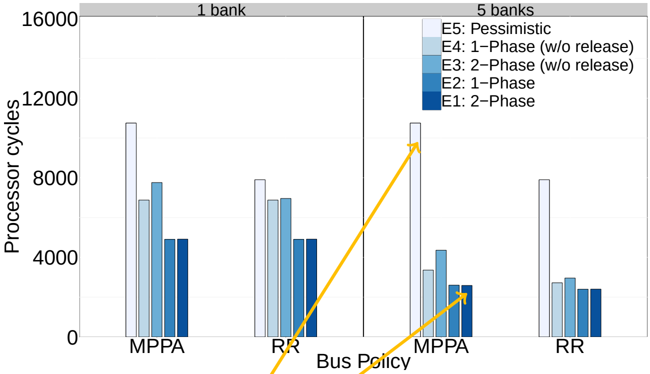

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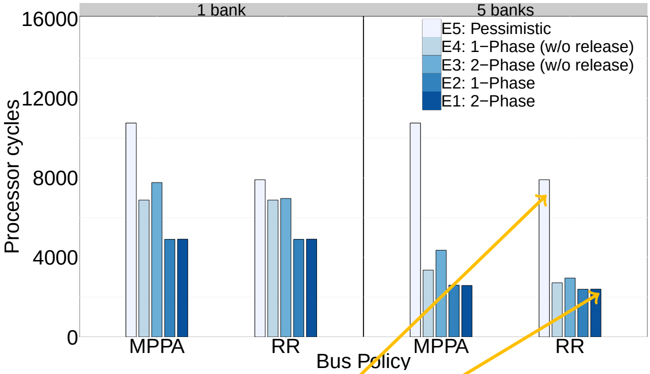

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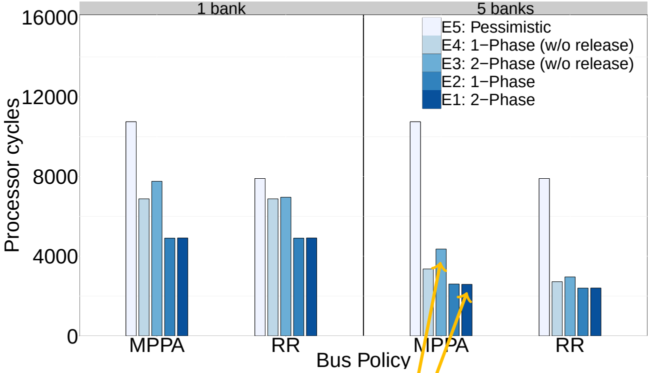

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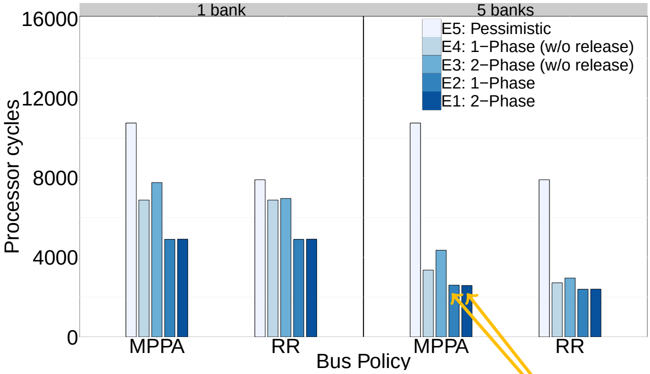

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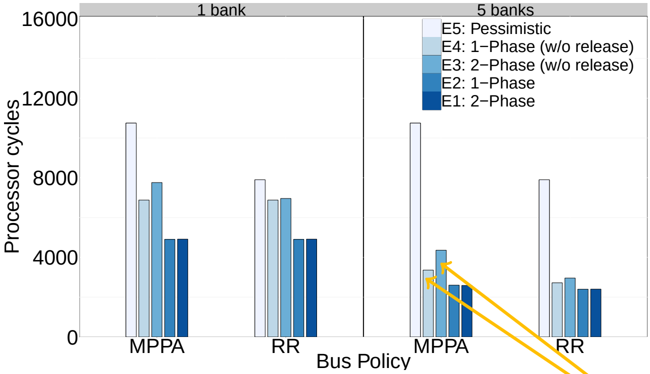

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Conclusion

- A response time analysis of SDF on the Kalray MPPA 256

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- A response time analysis of SDF on the Kalray MPPA 256
- Given:
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  - Mapping of Tasks
  - Execution Order

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- We compute:
  - Tight response times taking into account $\underline{\text{the interference}}$.
  - Release dates respecting the $\underline{\text{dependency constraints}}$.

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model of
the multi-level arbiter

Conclusion

- A response time analysis of SDF on the Kalray MPPA 256

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model of
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double fixed-point
algorithm

Conclusion

- A response time analysis of SDF on the Kalray MPPA 256
- Given:
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- We compute:
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  - Release dates respecting the dependency constraints.
- Not restricted to SDF

model of
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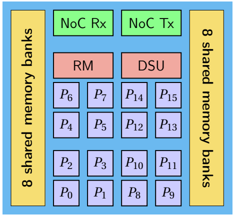
Future Work

- Model of the Resource Manager.



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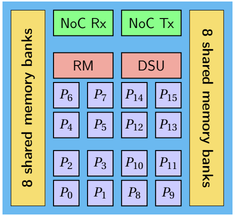
- Model of the Resource Manager.

tighter estimation of context switches and other interrupts



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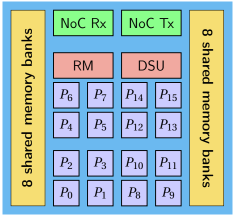

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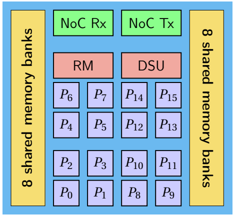
use the output of any NoC analysis



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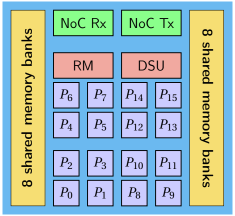
- Memory access pipelining.



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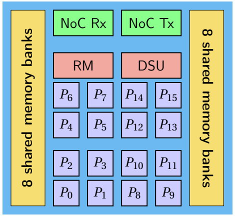
current assumption: bus delay is 10 cycles



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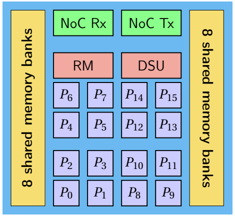
- Model Blocking and non-blocking accesses.


8 shared memory banks
NoC Rx
NoC Tx
RM
DSU
P_6 P_7 P_{14} P_{15}
P_4 P_5 P_{12} P_{13}
P_2 P_3 P_{10} P_{11}
P_0 P_1 P_8 P_9
8 shared memory banks

Future Work

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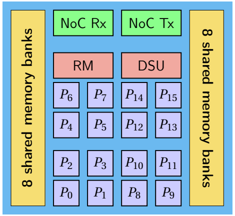

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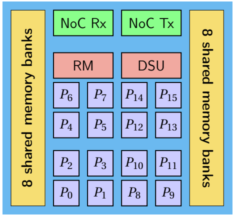


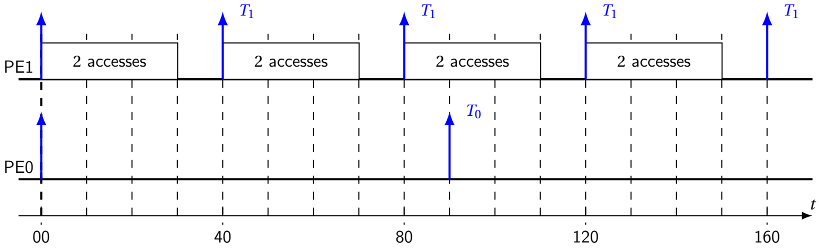
Questions?

BACKUP

Multicore Response Time Analysis

Example: Fixed Priority bus arbiter, PE1 > PE0

Bus access delay = 10



[1] Altmeyer et al., RTNS 2015

Multicore Response Time Analysis

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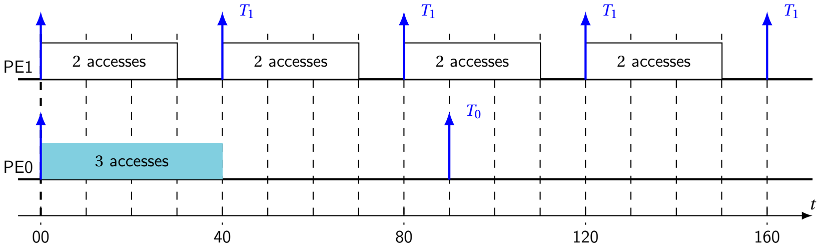
Bus access delay = 10



- Task of interest running on $PE0$:

  $R_0 = 10 + 3 \times 10$ (response time in isolation)

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Multicore Response Time Analysis

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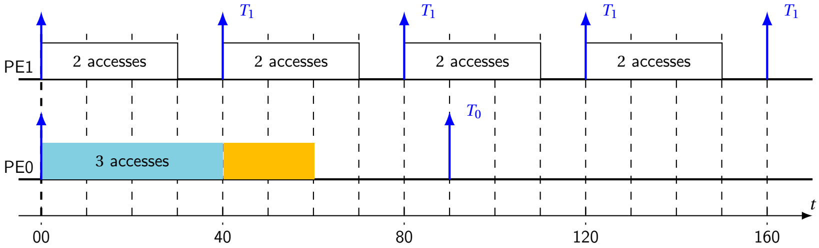

- Task of interest running on $PE0$:

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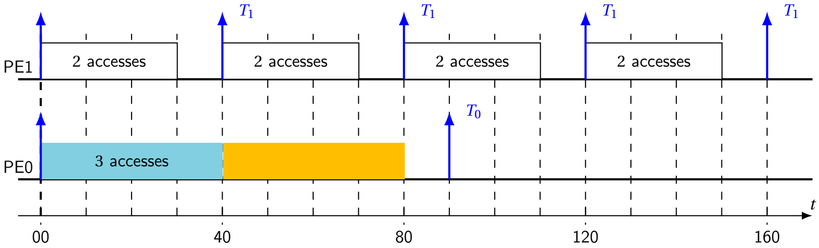
  $R_1 = 10 + 3 \times 10 + 2 \times 10 = 60$

[1] Altmeyer et al., RTNS 2015

Multicore Response Time Analysis

Example: Fixed Priority bus arbiter, PE1 > PE0
Bus access delay = 10



- Task of interest running on $PE0$:

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  $R_1 = 10 + 3 \times 10 + 2 \times 10 = 60$

  $R_2 = 10 + 3 \times 10 + 2 \times 10 + 2 \times 10 = 80$

[1] Altmeyer et al., RTNS 2015

Multicore Response Time Analysis

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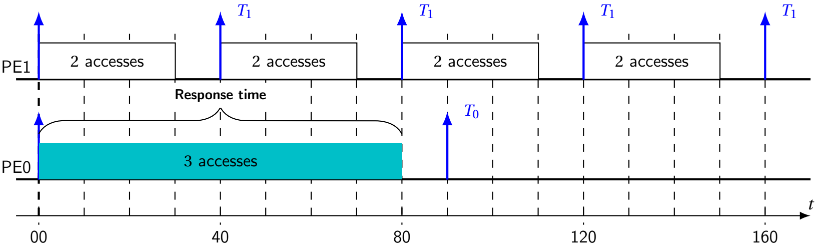

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  $R_0 = 10 + 3 \times 10$ (response time in isolation)

  $R_1 = 10 + 3 \times 10 + 2 \times 10 = 60$

  $R_2 = 10 + 3 \times 10 + 2 \times 10 + 2 \times 10 = 80$

  $R_3 = 10 + 3 \times 10 + 2 \times 10 + 2 \times 10 + 0 = 80$ (fixed-point)

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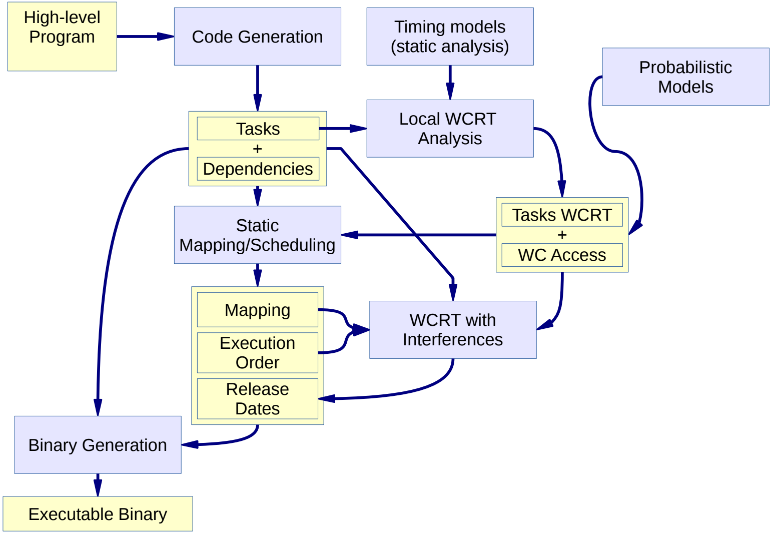
The Global Picture


High-level Program
Code Generation
Timing models (static analysis)
Probabilistic Models
Tasks
+
Dependencies
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