

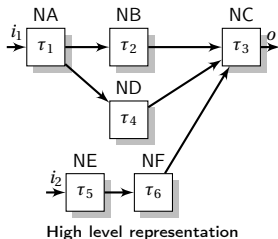
Response Time Analysis of Synchronous Data Flow Programs on a Many-Core Processor

Hamza Rihani, Matthieu Moy, Claire Maiza, Robert I. Davis, Sebastian Altmeyer

RTNS'16, October 19, 2016



Execution of Synchronous Data Flow Programs

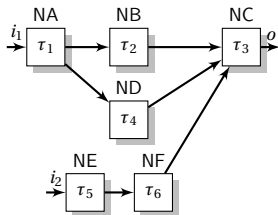


Single-core
code generation

static non-preemptive scheduling

```
int main_app(i1, i2)
{
    na = NA(i1);
    ne = NE(i2);
    nb = NB(na);
    nd = ND(na);
    nf = NF(ne);
    o = NC(nb, nd, nf);
    return o;
}
```

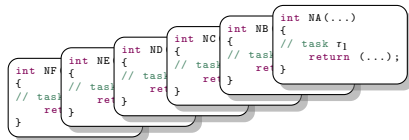
Execution of Synchronous Data Flow Programs



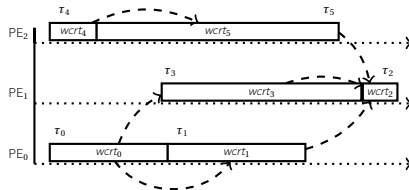
High level representation

Multi/Many-core

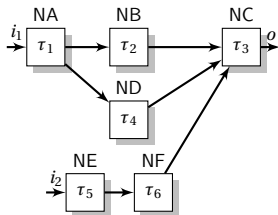
code generation



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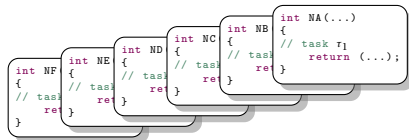


Execution of Synchronous Data Flow Programs



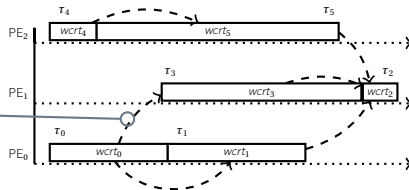
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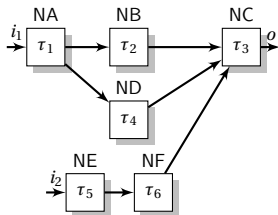


static non-preemptive scheduling

✓ Respect the dependency constraints



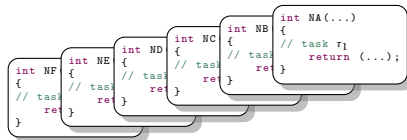
Execution of Synchronous Data Flow Programs



High level representation

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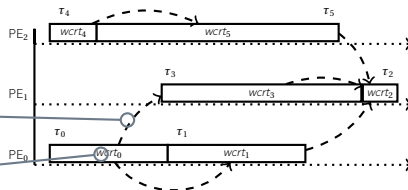
code generation



static non-preemptive scheduling

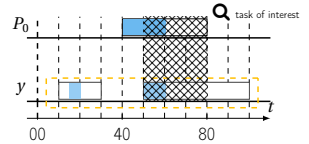
✓ Respect the dependency constraints

✓ Set the release dates to get precise upper bounds on the interference



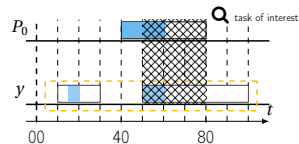
Contributions

- 1 Precise accounting for interference on shared resources in a many-core processor

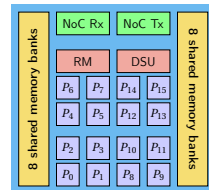


Contributions

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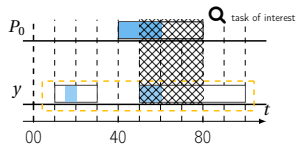


- 2 Model of a multi-level arbiter to the shared memory

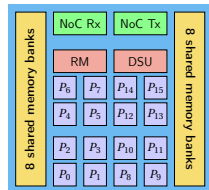


Contributions

- 1 Precise accounting for interference on shared resources in a many-core processor



- 2 Model of a multi-level arbiter to the shared memory



- 3 Response time and release dates analysis respecting dependencies.

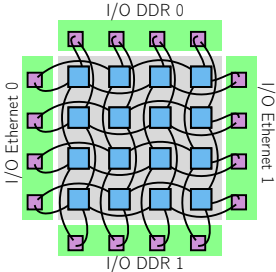
Outline

- 1 Motivation and Context
- 2 Models Definition
 - Architecture Model
 - Execution Model
 - Application Model
- 3 Multicore Response Time Analysis of SDF Programs
- 4 Evaluation
- 5 Conclusion and Future Work

Outline

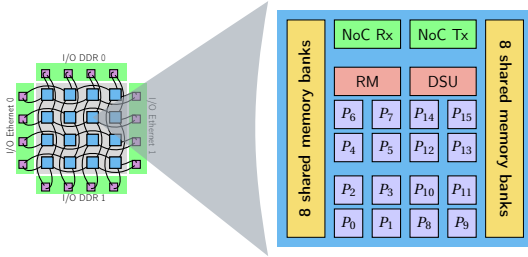
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Architecture Model



- Kalray MPPA 256 Bostan
- 16 compute clusters + 4 I/O clusters
- Dual NoC

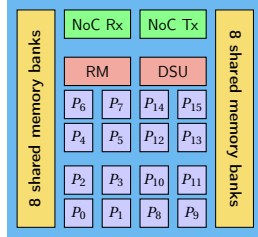
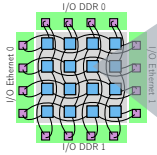
Architecture Model



Per cluster:

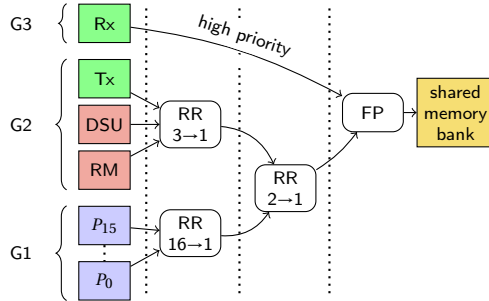
- 16 cores + 1 Resource Manager
- NoC Tx, NoC Rx, Debug Unit
- 16 shared memory banks per cluster (total 2 MB)

Architecture Model

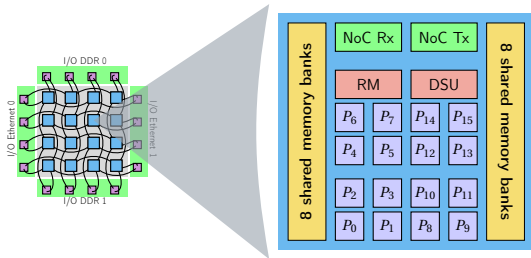


Per cluster:

- 16 cores + 1 Resource Manager
- NoC Tx, NoC Rx, Debug Unit
- 16 shared memory banks per cluster (total 2 MB)
- Multi-level bus arbiter per memory bank

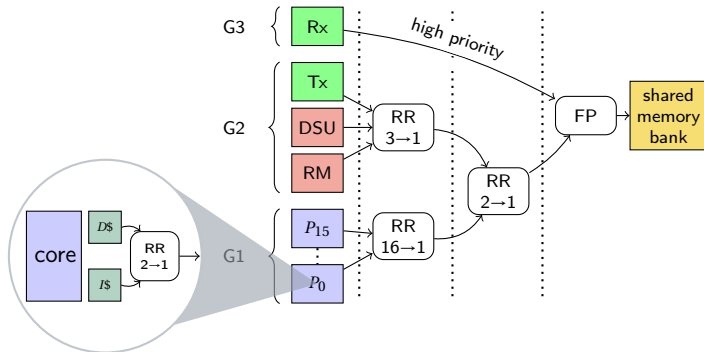


Architecture Model

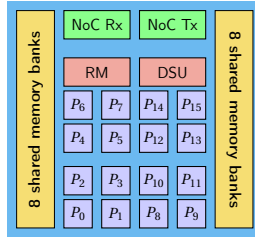
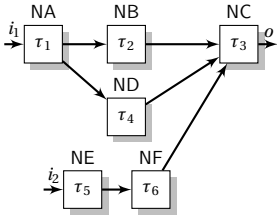


Per cluster:

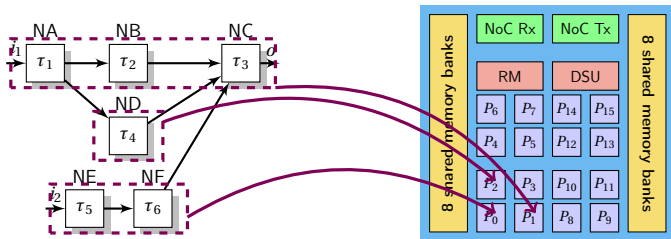
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Execution Model

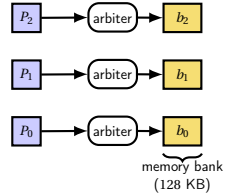
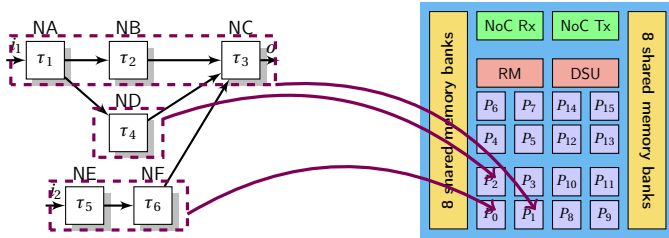


Execution Model



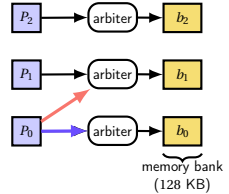
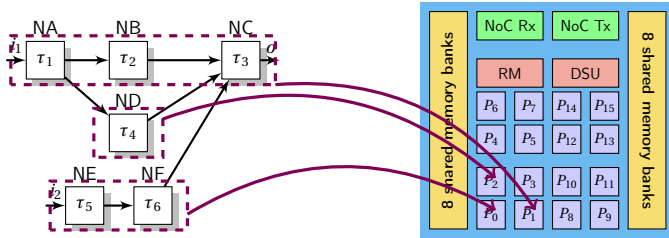
- Tasks mapping on cores
- Static non-preemptive scheduling

Execution Model



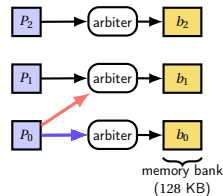
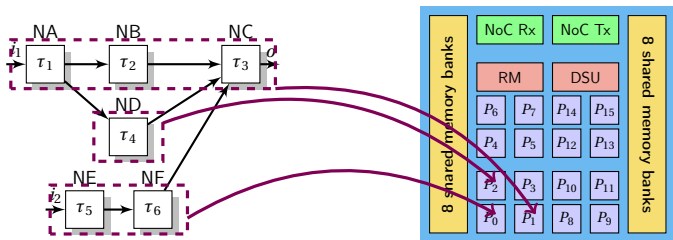
- Tasks mapping on cores
- Static non-preemptive scheduling
- Spatial Isolation
 - different tasks go to different memory banks

Execution Model



- Tasks mapping on cores
- Static non-preemptive scheduling
- Spatial Isolation
 - different tasks go to different memory banks
- Interference from communications

Execution Model

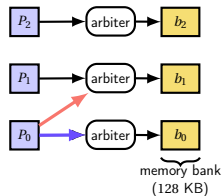
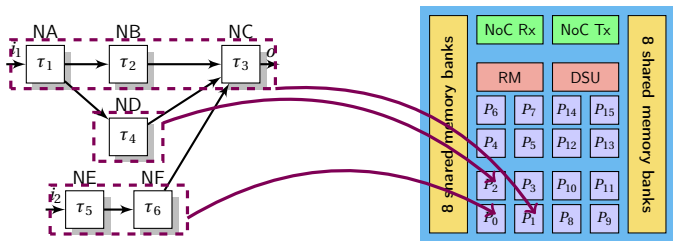


- Tasks mapping on cores
- Static non-preemptive scheduling
- Spatial Isolation
 - different tasks go to different memory banks
- Interference from communications
- Execution model:
 - execute in a “local” bank
 - write to a “remote” bank

Single phase: execute *and* write data.



Execution Model



- Tasks mapping on cores
- Static non-preemptive scheduling
- Spatial Isolation
 - different tasks go to different memory banks
- Interference from communications
- Execution model:
 - execute in a “local” bank
 - write to a “remote” bank

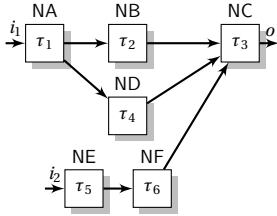
Single phase: execute *and* write data.



Two phases: execute *then* write data.

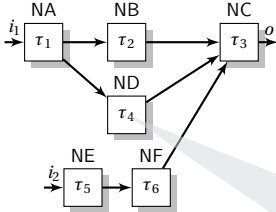


Application Model



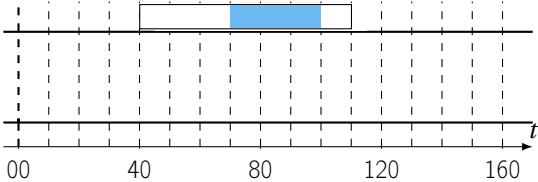
- Direct Acyclic Task Graph
- Mono-rate (or at least harmonic rates)
- Fixed mapping and execution order

Application Model

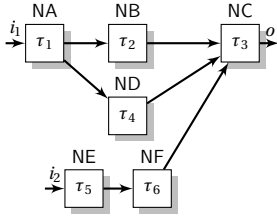


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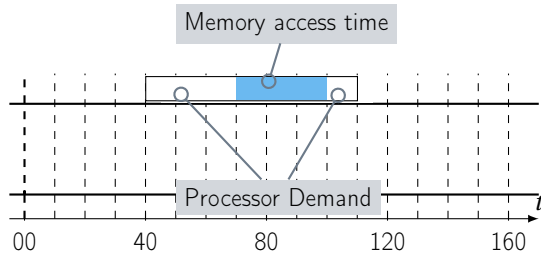
Each task τ_i :



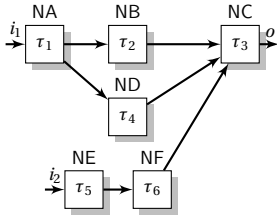
Application Model



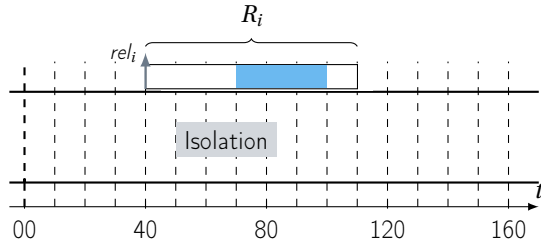
- Direct Acyclic Task Graph
 - Mono-rate (or at least harmonic rates)
 - Fixed mapping and execution order
- Each task τ_i :**
- Processor Demand, Memory Demand



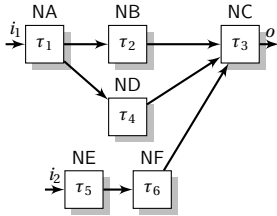
Application Model



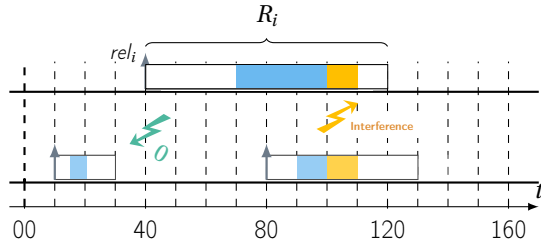
- Direct Acyclic Task Graph
 - Mono-rate (or at least harmonic rates)
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- Each task τ_i :**
- Processor Demand, Memory Demand
 - Release date (rel_i), response time (R_i)



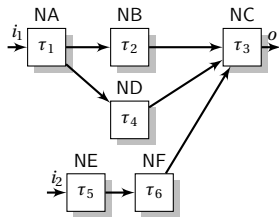
Application Model



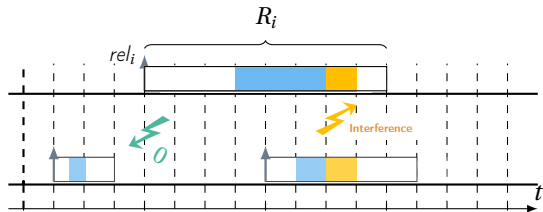
- Direct Acyclic Task Graph
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 - Release date (rel_i), response time (R_i)



Application Model



- Direct Acyclic Task Graph
 - Mono-rate (or at least harmonic rates)
 - Fixed mapping and execution order
- Each task τ_i :**
- Processor Demand, Memory Demand
 - Release date (rel_i), response time (R_i)




- 🔍 Find R_i (including the interference)
- 🔍 Find rel_i respecting precedence constraints

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Response Time Analysis

- Response Time

$$R = PD + I^{BUS}(R)$$


Response Time Analysis


- Response Time
- Processor Demand

$$R = PD + I^{BUS}(R)$$


Response Time Analysis

$$R = PD + I^{BUS}(R)$$

- Response Time
- Processor Demand
- Bus Interference
(given a model of the bus arbiter)

The diagram consists of the equation $R = PD + I^{BUS}(R)$ at the top. Below it is a bulleted list. Three green arrows originate from the list items and point to the corresponding terms in the equation: one from 'Response Time' to 'R', one from 'Processor Demand' to 'PD', and one from 'Bus Interference' to ' $I^{BUS}(R)$ '.

Response Time Analysis

$$R = PD + I^{BUS}(R) + I^{PROC}(R) + I^{DRAM}(R)$$

- Response Time

- Processor Demand

- Bus Interference

- (given a model of the bus arbiter)*

- Interference from preempting tasks

- (no preemption: $I^{PROC} = 0$)*

- Interference from DRAM refreshes

- (out of scope. $I^{DRAM} = 0$)*

Response Time Analysis

$$R = PD + I^{BUS}(R) + I^{PROC}(R) + I^{DRAM}(R)$$

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- Recursive formula \Rightarrow fixed-point algorithm.

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- Multiple shared resources (memory banks)

Response Time Analysis

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- Response Time

- Processor Demand

- Bus Interference

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$$I^{BUS}(R) = \sum_{b \in B} I_b^{BUS}(R)$$

where B : a set of memory banks

Response Time Analysis

$$R = PD + I^{BUS}(R) + I^{PROC}(R) + I^{DRAM}(R)$$

- Response Time

- Processor Demand

- Bus Interference

(given a model of the bus arbiter)

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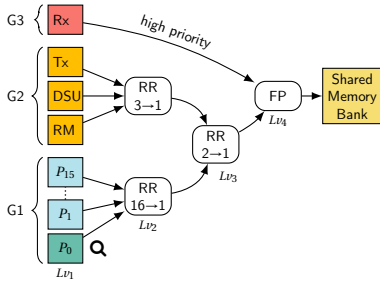
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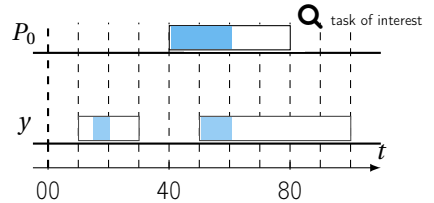


Requires a model of the bus arbiter

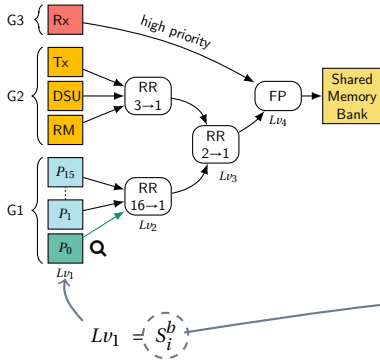
Model of the MPPA Bus



I_b^{BUS} : delay from all accesses + concurrent ones



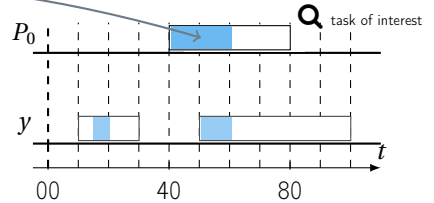
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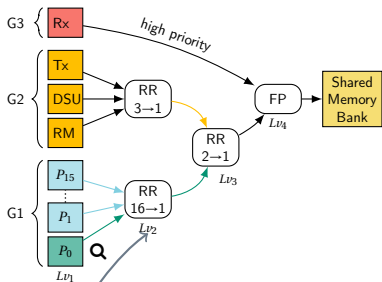
I_b^{BUS} : delay from all accesses + concurrent ones

S_i^b : number of accesses of task τ_i to bank b

$S_i^b =$ Memory Demand to bank b



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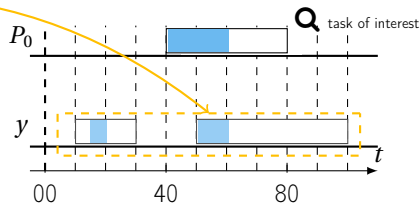
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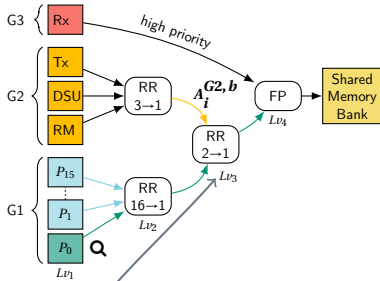
$A_i^{y,b}$: number of concurrent accesses from core y to bank b

$$Lv_1 = S_i^b$$

$$Lv_2 = Lv_1 + \sum_{y=1}^{15} \min(A_i^{y,b}, Lv_1)$$



Model of the MPPA Bus

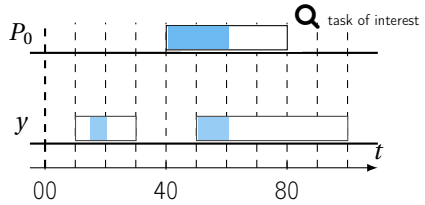


I_b^{BUS} : delay from all accesses + concurrent ones
 S_i^b : number of accesses of task τ_i to bank b
 $S_i^b = \text{Memory Demand to bank } b$
 $A_i^{y,b}$: number of concurrent accesses from core y to bank b

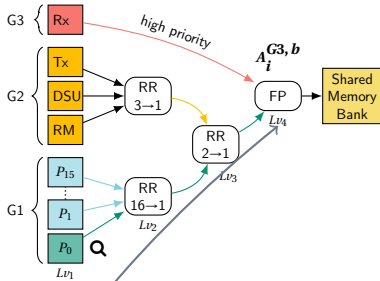
$$Lv_1 = S_i^b$$

$$Lv_2 = Lv_1 + \sum_{y=1}^{15} \min(A_i^{y,b}, Lv_1)$$

$$Lv_3 = Lv_2 + \min(A_i^{G2,b}, Lv_2)$$



Model of the MPPA Bus



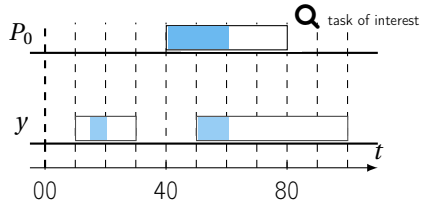
I_b^{BUS} : delay from all accesses + concurrent ones
 S_i^b : number of accesses of task τ_i to bank b
 $S_i^b = \text{Memory Demand to bank } b$
 $A_i^{y,b}$: number of concurrent accesses from core y to bank b

$$Lv_1 = S_i^b$$

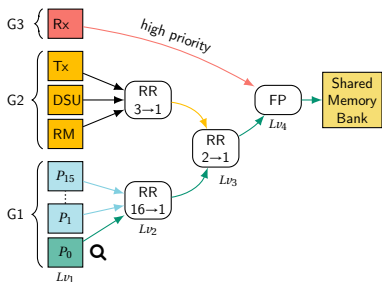
$$Lv_2 = Lv_1 + \sum_{y=1}^{15} \min(A_i^{y,b}, Lv_1)$$

$$Lv_3 = Lv_2 + \min(A_i^{G2,b}, Lv_2)$$

$$Lv_4 = Lv_3 + A_i^{G3,b}$$



Model of the MPPA Bus



I_b^{BUS} : delay from all accesses + concurrent ones

S_i^b : number of accesses of task τ_i to bank b

$S_i^b = \text{Memory Demand to bank } b$

$A_i^{y,b}$: number of concurrent accesses from core y to bank b

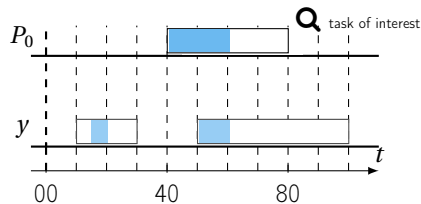
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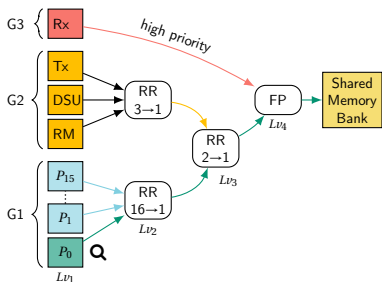
$$Lv_3 = Lv_2 + \min(A_i^{G2,b}, Lv_2)$$

$$Lv_4 = Lv_3 + A_i^{G3,b}$$

$$I_b^{BUS} = Lv_4 \times \text{Bus Delay}$$



Model of the MPPA Bus



I_b^{BUS} : delay from all accesses + concurrent ones

S_i^b : number of accesses of task τ_i to bank b

$S_i^b =$ Memory Demand to bank b

$A_i^{y,b}$: number of concurrent accesses from core y to bank b

$A_i^{y,b} = \sum$ overlapping concurrent accesses

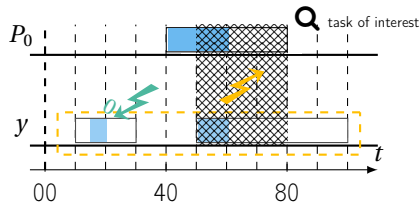
$$Lv_1 = S_i^b$$

$$Lv_2 = Lv_1 + \sum_{y=1}^{15} \min(A_i^{y,b}, Lv_1)$$

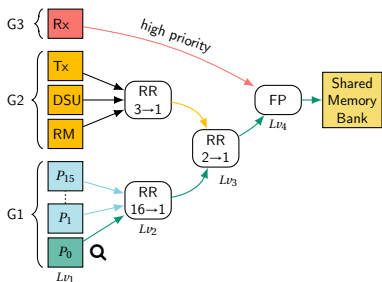
$$Lv_3 = Lv_2 + \min(A_i^{G2,b}, Lv_2)$$

$$Lv_4 = Lv_3 + A_i^{G3,b}$$

$$I_b^{BUS} = Lv_4 \times \text{Bus Delay}$$



Model of the MPPA Bus



I_b^{BUS} : delay from all accesses + concurrent ones

S_i^b : number of accesses of task τ_i to bank b

$S_i^b =$ Memory Demand to bank b

$A_i^{y,b}$: number of concurrent accesses from core y to bank b

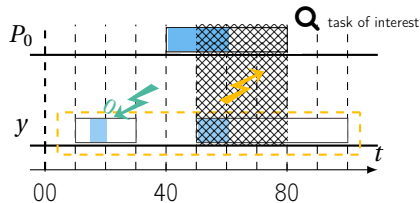
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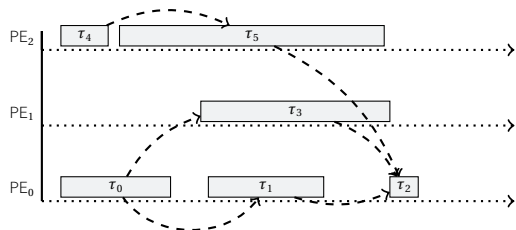
$$Lv_4 = Lv_3 + A_i^{G3,b}$$



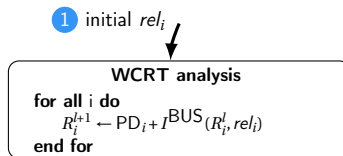
$A_i^{y,b}$ depends on rel_i and R_i

$$I_b^{BUS} = Lv_4 \times \text{Bus Delay}$$

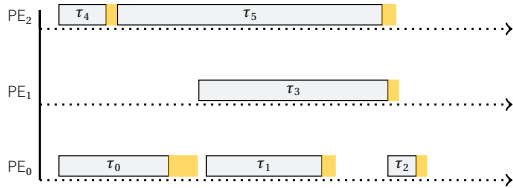
Response Time Analysis with Dependencies



1 Start with initial release dates.



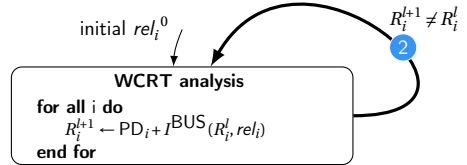
Response Time Analysis with Dependencies



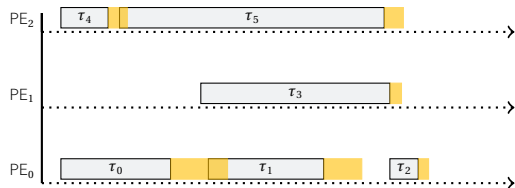
1 Start with initial release dates.

2 Compute response times

...



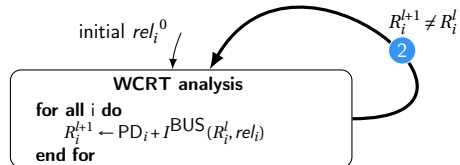
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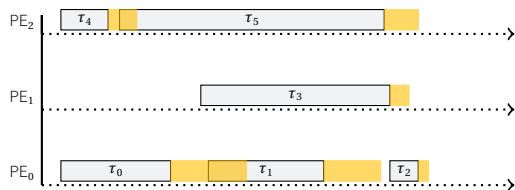
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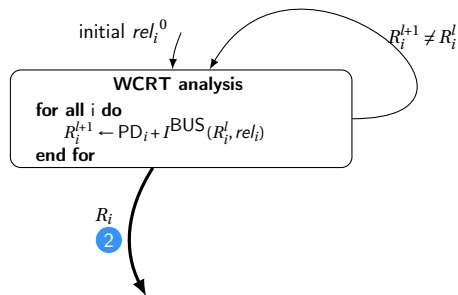
... ..



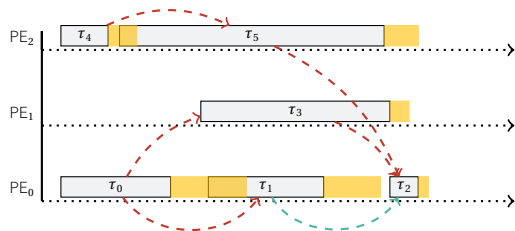
Response Time Analysis with Dependencies



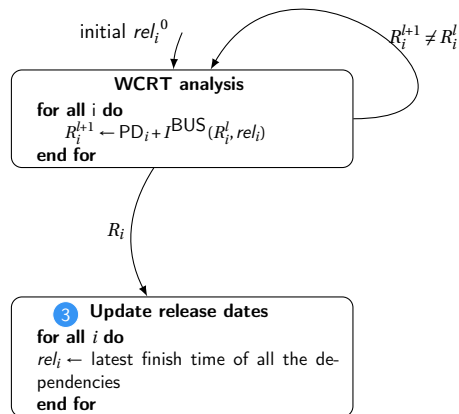
- 1 Start with initial release dates.
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... .. a fixed-point is reached!



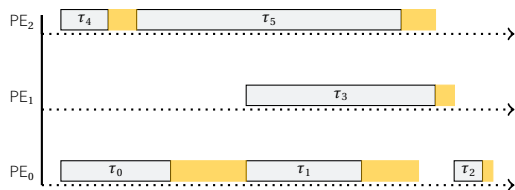
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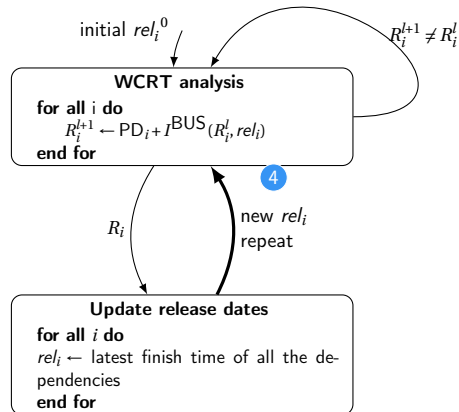
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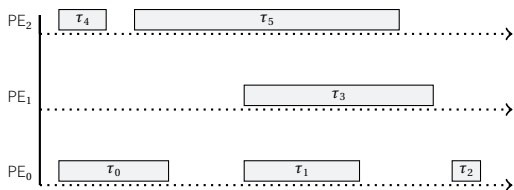
Response Time Analysis with Dependencies



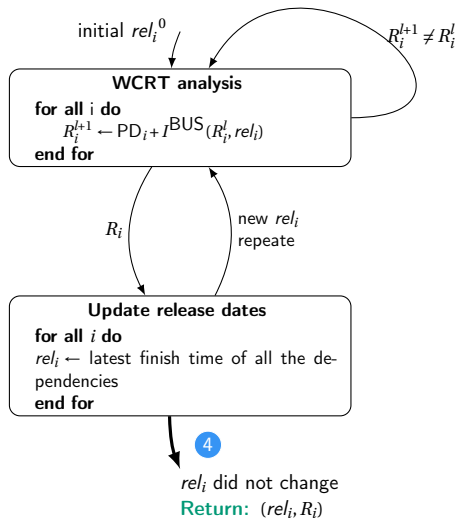
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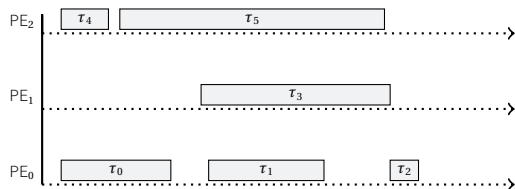
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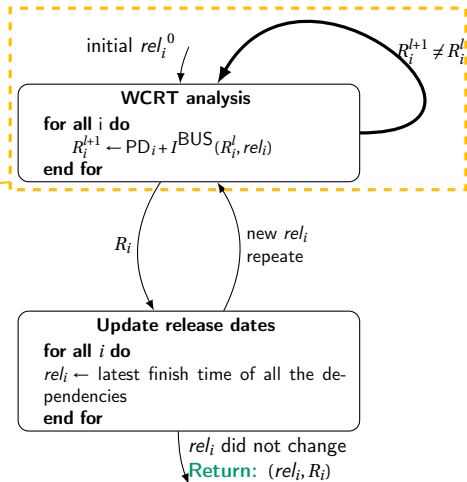
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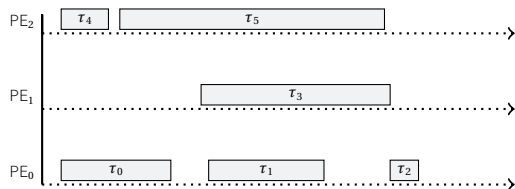
Convergence Toward a Fixed-point



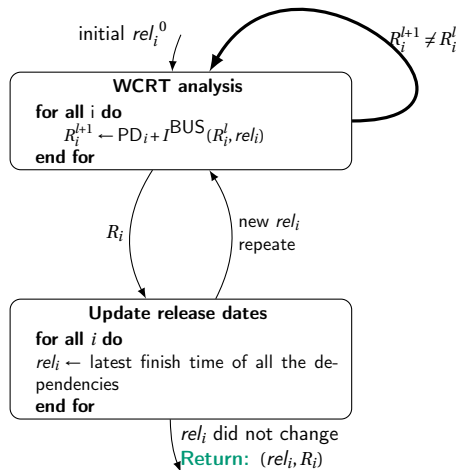
- Convergence of the 1st fixed-point iteration:



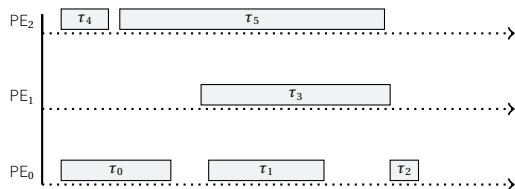
Convergence Toward a Fixed-point



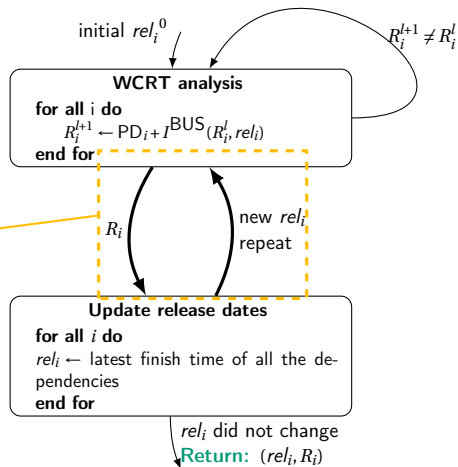
- Convergence of the 1st fixed-point iteration:
 - Monotonic and bounded ✓



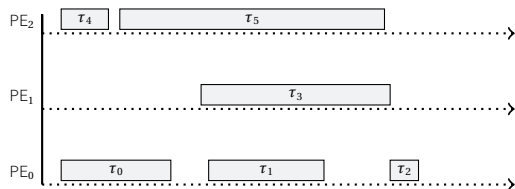
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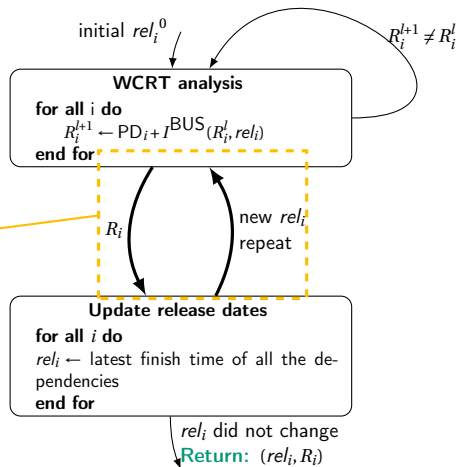
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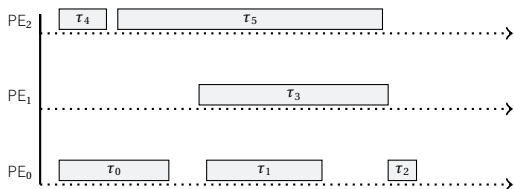
Convergence Toward a Fixed-point



- Convergence of the 1st fixed-point iteration:
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- Convergence of the 2nd fixed-point iteration:
 - no monotonicity: R_i and rel_i may grow or shrink at each iteration. ?



Convergence Toward a Fixed-point



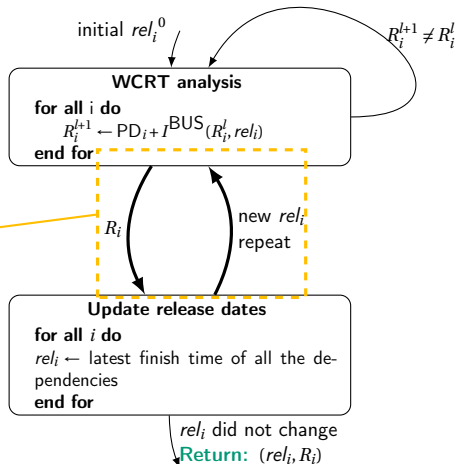
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Theorem

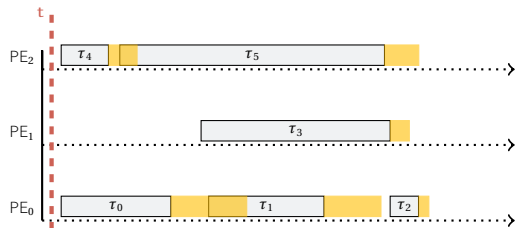
At each iteration, at least one task finds its final release date.

Full proof in our technical report:

<http://www-verimag.imag.fr/TR/TR-2016-1.pdf>



Convergence Toward a Fixed-point



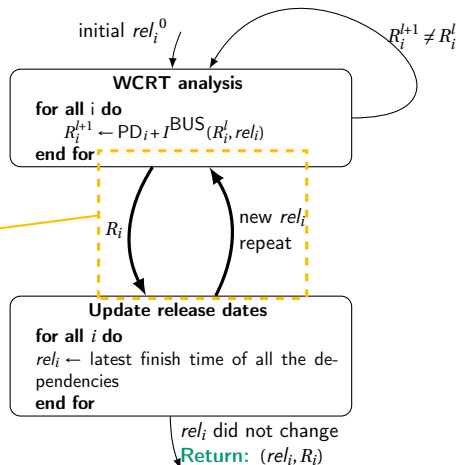
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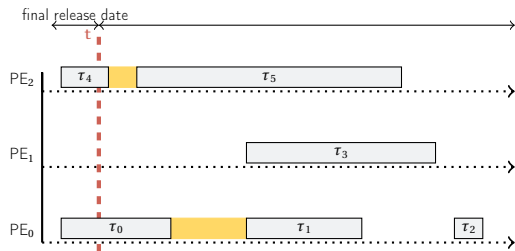
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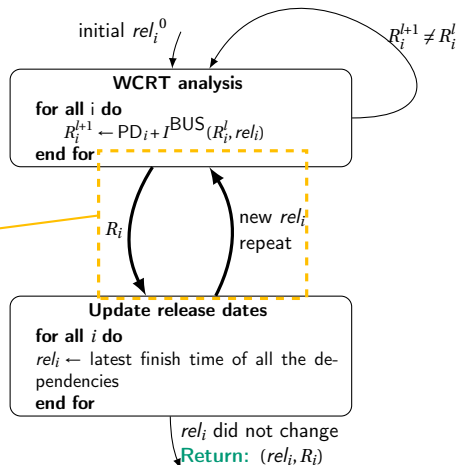
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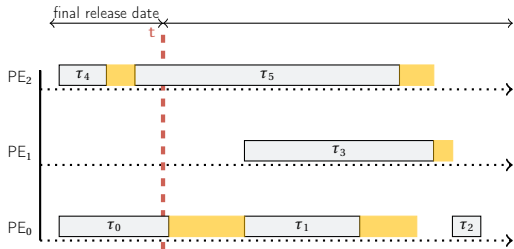
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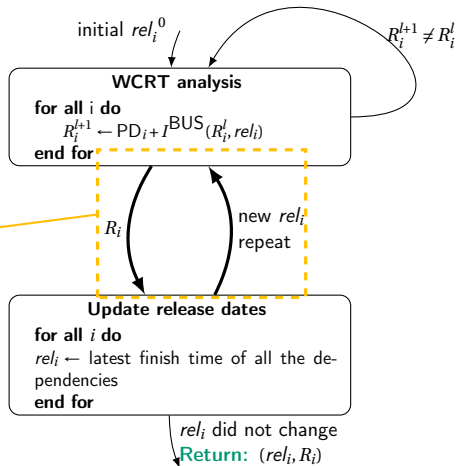
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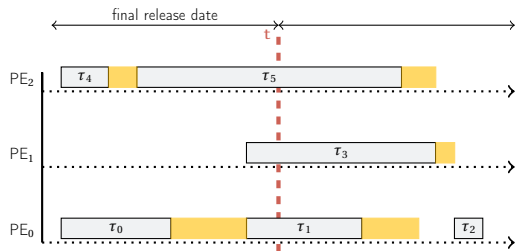
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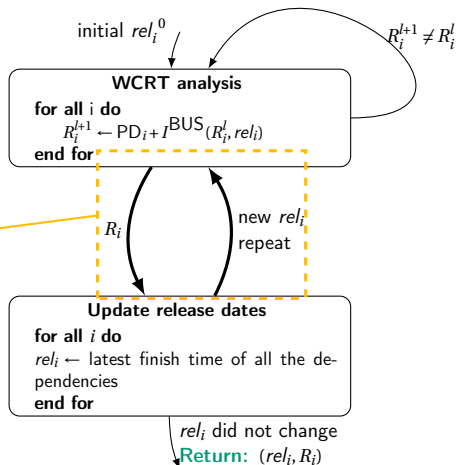
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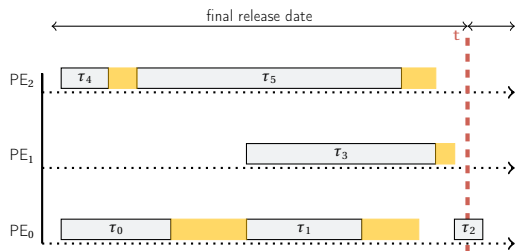
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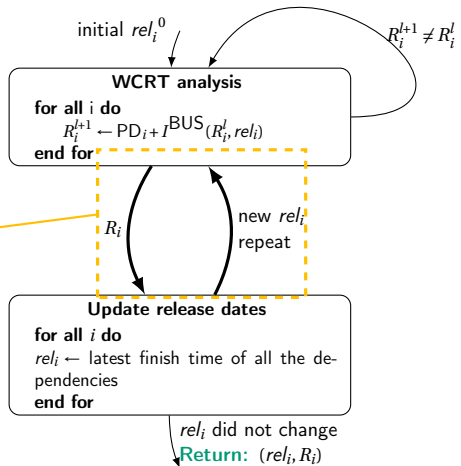
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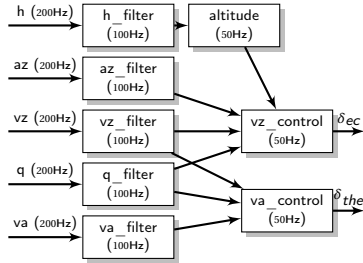
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Outline

- 1 Motivation and Context
- 2 Models Definition
 - Architecture Model
 - Execution Model
 - Application Model
- 3 Multicore Response Time Analysis of SDF Programs
- 4 Evaluation
- 5 Conclusion and Future Work

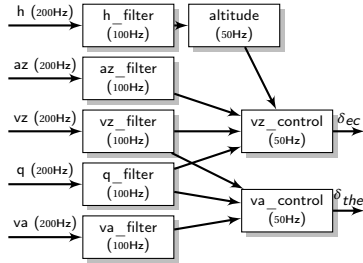
Evaluation: ROSACE Case Study ¹



- Flight management system controller

¹ Pagetti et al., RTAS 2014

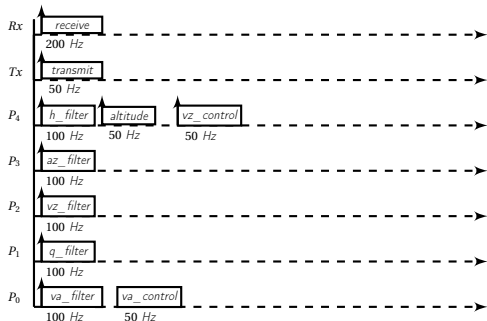
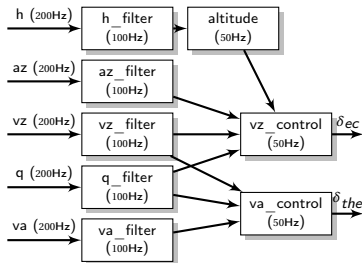
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- Flight management system controller
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Evaluation: ROSACE Case Study ¹



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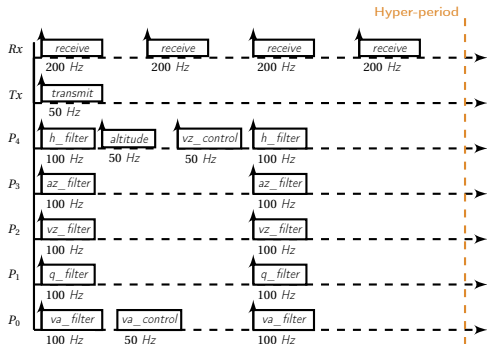
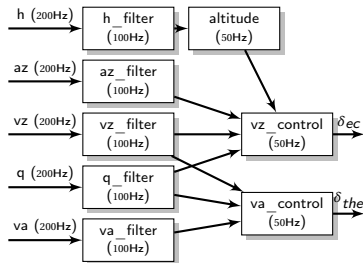
Tasks are mapped on 5 cores

Debug Support Unit is disabled

Context switches are over-approximated constants

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va_filter	301	23
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Table: Task profiles of the FMS controller

- Profile obtained from measurements

Evaluation: ROSACE Case Study

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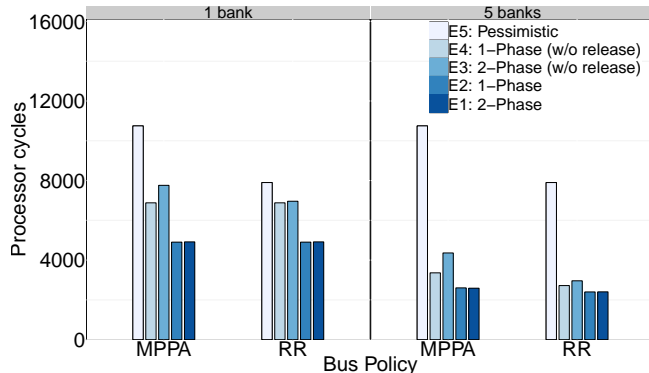
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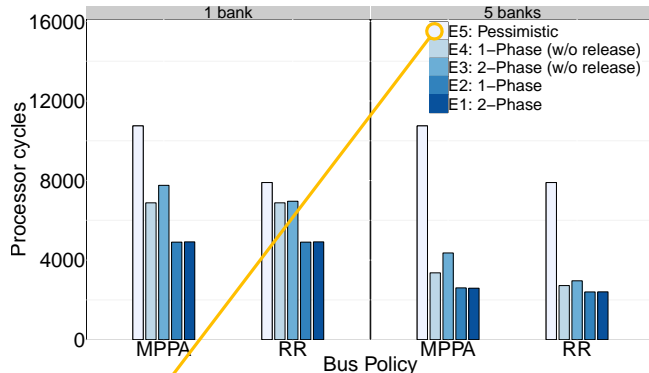
Experiments: Find the smallest schedulable hyper-period

Evaluation: Experiments



Smallest schedulable hyper-period

Evaluation: Experiments

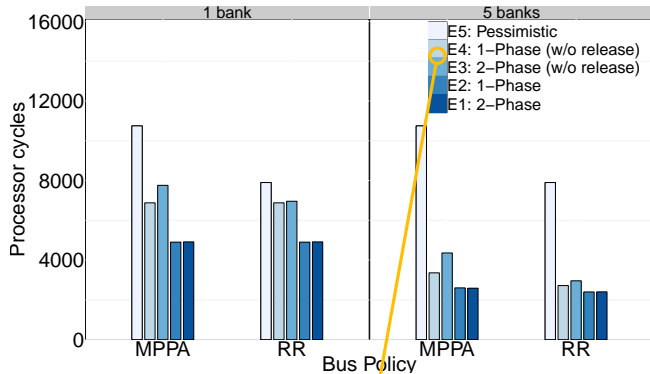


- Pessimistic assumption: High priority tasks are bounded by 1 access per bank

Smallest schedulable hyper-period

E5: All accesses interfere

Evaluation: Experiments



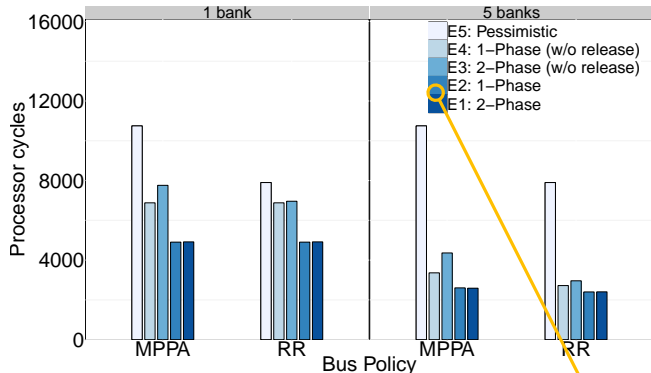
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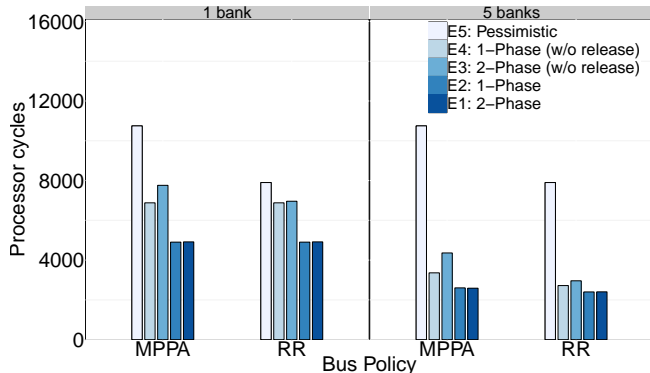
E2, E1: Our approach. We use the release dates

Evaluation: Experiments

1-Phase model



2-Phase model



- Pessimistic assumption: High priority tasks are bounded by 1 access per bank
- Phases are modeled as sub-tasks

Smallest schedulable hyper-period

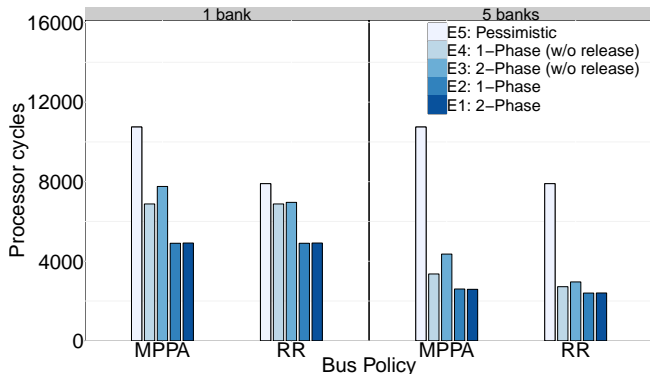
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Taking into account the memory banks improves the analysis with a factor in [1.77,2.52]



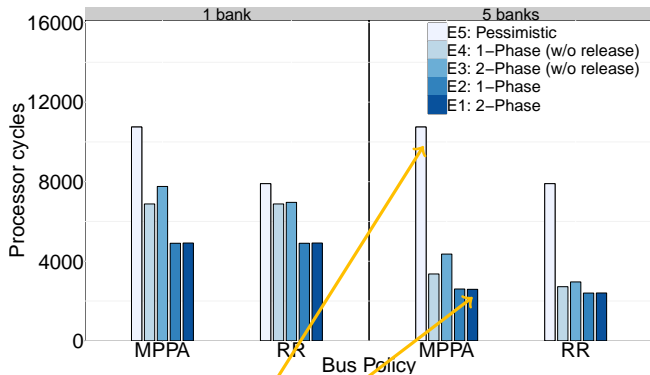
Smallest schedulable hyper-period

	E5/E1	E5/E2	E3/E1	E4/E2	E2/E1	E4/E3
MPPA	4.15	4.12	1.68	1.29	~1.01	0.77
RR	3.3	3.29	1.24	1.13	~1.01	0.91

Speedup factors

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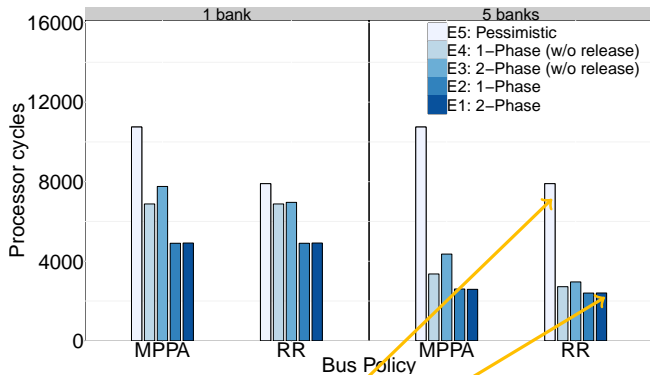
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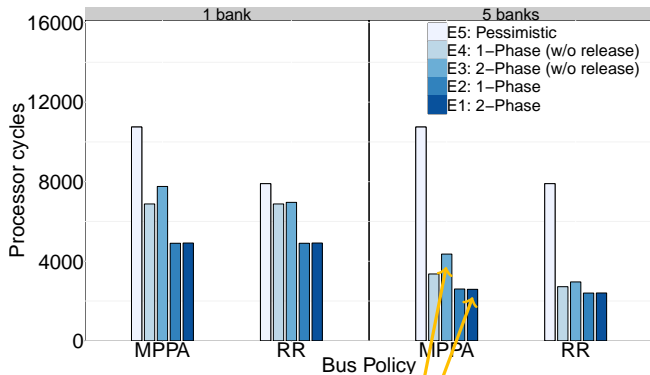
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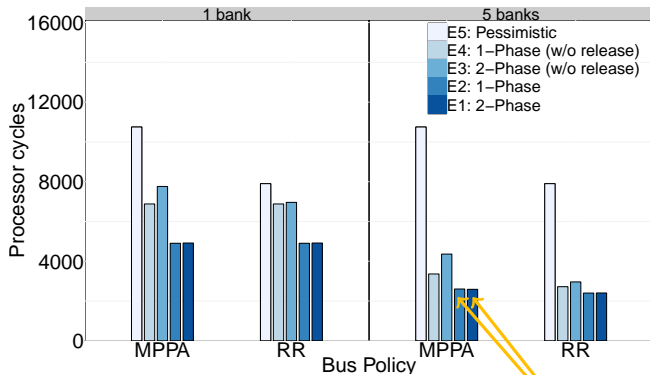
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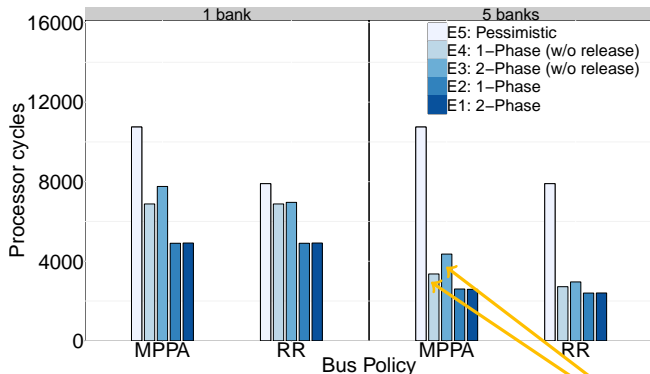


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Conclusion

- A response time analysis of SDF on the Kalray MPPA 256

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- Given:
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 - Tight response times taking into account the interference.
 - Release dates respecting the dependency constraints.

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model of
the multi-level arbiter

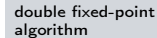
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double fixed-point
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Conclusion

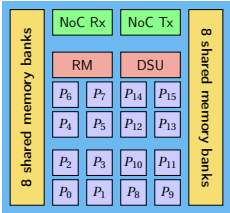
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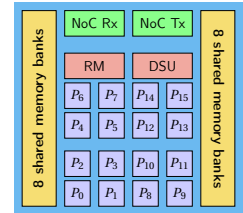
Future Work

- Model of the Resource Manager.



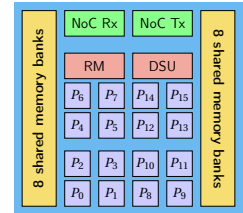
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- Model of the Resource Manager. tighter estimation of context switches and other interrupts



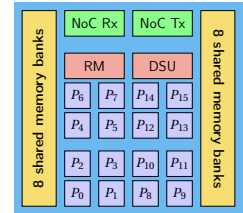
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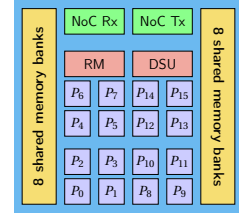
Future Work

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- Model of the NoC accesses. use the output of any NoC analysis



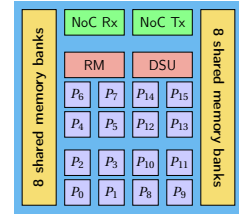
Future Work

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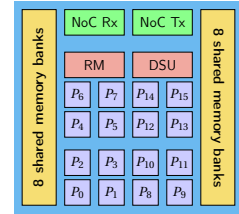
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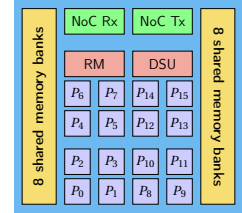
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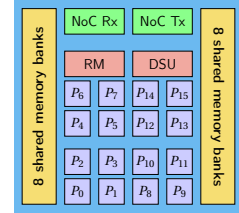
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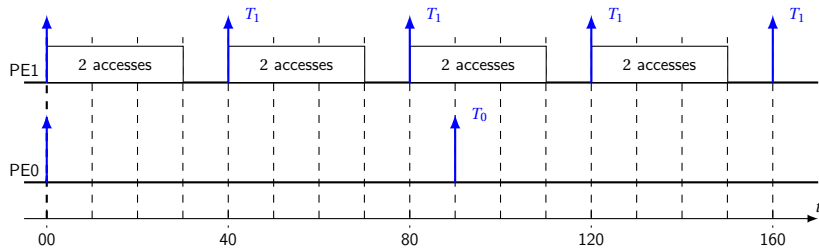


Questions?

BACKUP

Multicore Response Time Analysis

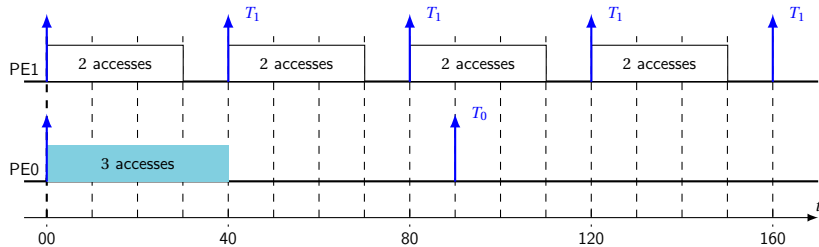
Example: Fixed Priority bus arbiter, $PE1 > PE0$
Bus access delay = 10



Multicore Response Time Analysis

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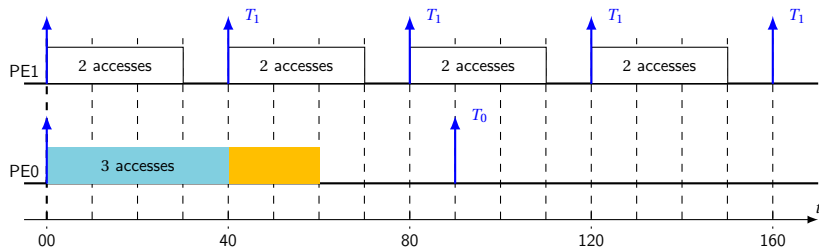


- Task of interest running on $PE0$:
 $R_0 = 10 + 3 \times 10$ (response time in isolation)

Multicore Response Time Analysis

Example: Fixed Priority bus arbiter, $PE1 > PE0$

Bus access delay = 10



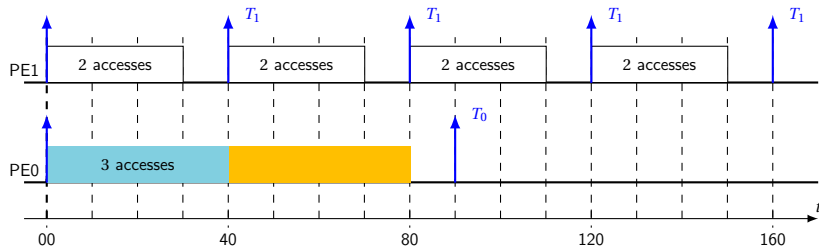
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$$R_1 = 10 + 3 \times 10 + 2 \times 10 = 60$$

Multicore Response Time Analysis

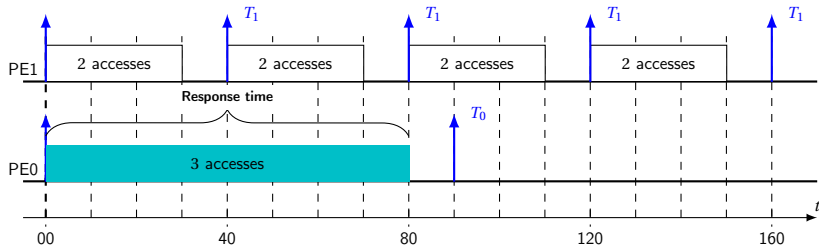
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 $R_0 = 10 + 3 \times 10$ (response time in isolation)
 $R_1 = 10 + 3 \times 10 + 2 \times 10 = 60$
 $R_2 = 10 + 3 \times 10 + 2 \times 10 + 2 \times 10 = 80$

Multicore Response Time Analysis

Example: Fixed Priority bus arbiter, $PE1 > PE0$
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- Task of interest running on $PE0$:

$$R_0 = 10 + 3 \times 10 \text{ (response time in isolation)}$$

$$R_1 = 10 + 3 \times 10 + 2 \times 10 = 60$$

$$R_2 = 10 + 3 \times 10 + 2 \times 10 + 2 \times 10 = 80$$

$$R_3 = 10 + 3 \times 10 + 2 \times 10 + 2 \times 10 + 0 = 80 \text{ (fixed-point)}$$

