Degree Examinations 2014 – 2015

DEPARTMENT OF COMPUTER SCIENCE

Computer Systems Architecture

Time allowed: two hours

Calculators may not be used in this examination.

Candidates should answer Question 1, and any two others from Questions 2, 3 and 4.

Do not use red ink.

Q1. [20 Marks]

(i) [10 marks] Examine the logic circuit shown in figure 1.
   a. [3 marks] What are the three logic gates used in this circuit?
   b. [4 marks] Write out the truth table for this circuit describing its input to output behaviour i.e. the relationship between its inputs A and B, and its output Z.
   c. [1 mark] If each logic gate has a propagation delay of 10 ns, what is the critical path delay?
   d. [2 mark] What logic function does this circuit implement?

![Logic Circuit Diagram]

Figure 1: Logic circuit

(ii) [10 marks] An imaginary processor has the following hardware specification:
   • 8bit data bus
   • 8bit address bus
   • 1 general purpose register call the accumulator (ACC)

Answer the following questions, state any assumptions taken about this processor’s architecture.

   a. [2 mark] Why does only having one general purpose register simplify the instruction format?
   b. [2 mark] What is the disadvantage of only having one general purpose register?

Briefly describe what bit fields are required within an instruction to encode the following functionality:

   c. [2 mark] 14 different instructions
   d. [2 mark] Immediate addressing e.g. ADD ACC, 0x10 add the constant 0x10 to the accumulator, store the result in the accumulator.
   e. [2 mark] If multiple general purpose registers were added to this processor’s architecture what modifications would need to be made to its instruction format?
Figure 2: PicoBlaze processor architecture

(i) [24 marks] Examine the block diagram shown in figure 2.
   a. [12 marks] Briefly describe the function of each block.
   b. [12 marks] This diagram illustrates the internal architecture of the PicoBlaze processor. A program to be executed on this processor has been implemented as a main program and an interrupt service routine. When an interrupt occurs, describe the step by step sequence of actions that are performed in this architecture to implement a context switch from the main program to the interrupt service routine and back again.

(ii) [4 marks] Convert the following numbers into an unsigned 8 bit binary representation. State any assumptions you make and show all working i.e. intermediate stages or results.
   a. $102_5$
   b. $33_6$

Continued...
(iii) [6 marks] Using the binary values calculated in section (ii) perform the following calculations using binary arithmetic. Show all working i.e. intermediate stages or results.
   a. $33_6 + 102_6$
   b. $102_6 + (-33_6)$

(iv) [6 marks] When using a two’s complement binary representation how do you determine if an overflow has occurred? Illustrate your answer using an appropriate example.
Q3. [40 Marks]

(i) [24 marks] A Picoblaze system with the instruction set given in Appendix A is used to process data stored in external memory. A set of 64 numbers ranging in value between -20 and +20 are stored in memory, starting at address 0x10.

   a. [6 marks] Draw a flowchart of a program that will replace each of the 64 numbers by the original number multiplied by 2. You may assume these numbers are represented using the two’s complement number format.

   b. [6 marks] Translate your flowchart for part (a) into an assembly language program using the PicoBlaze instruction set. Your answer should refer to each statement in the program, describing its function and purpose within the program.

   c. [4 marks] Sketch a flowchart segment to indicate how you would adapt this program so that it only multiplies positive numbers by 2 and leaves negative numbers unaltered.

   d. [4 marks] Translate your flowchart for part (c) into an assembly language program using the PicoBlaze instruction set. Your answer should refer to each statement in the program, describing its function and purpose within the program.

   e. [4 marks] What problem could occur if each number is multiplied by 8? Briefly describe how you would solve this problem and any possible impact on how information is stored in the processor’s registers or memory.

(ii) [4 marks] What is the relationship between the width of a processor’s address bus and data bus with the size of its memory i.e. the number of bits that can be stored in memory?

(iii) [8 marks] Describe a typical fetch-decode-execute cycle with reference to an instruction that performs the bitwise logical AND function on two register values. State any assumptions you make.

(iv) [4 marks] Briefly describe the three main programming language classifications used in a typical computer.
Q4. [40 Marks]

(i) [20 marks] A common method for restricting access to shared resources is through the use of a special protected variable called a semaphore. A simple assembly language implementation is shown in figure 3.

   a. [12 marks] Explain how these Picoblaze subroutines operate. The Picoblaze instruction set is given in the Appendix A. Your answer should refer to each statement in the program, describing its function and purpose within the program.
   
   b. [4 marks] Briefly describe how these subroutines could be used to control access to a shared memory mapped device.
   
   c. [4 marks] Using your description from part (b) extend your discussion to show how errors may occur within a program if a semaphore is not used.

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Figure 3: semaphore subroutines
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(ii) [8 marks] Briefly describe the difference between a multi-processor based system and a multi-threaded based system. Give one advantage and disadvantage of a multi-processor based system over a multi-threaded based system.

(iii) [8 marks] An algorithm within a program can be implemented as either a single-threaded process, or as a multi-threaded process. What are the possible advantages and disadvantages in implementing an algorithm as a multi-threaded process over a single-threaded process?

(iv) [4 marks] A process contains two threads: Task_A and Task_B. Task_A has a priority level of 20, whilst Task_B has a priority level of 10. How will an operating system execute these programs. State any assumptions you make.
Appendix A: PicoBlaze Instruction Set

Program Control Group

JUMP aa
JUMP Z,aa
JUMP NZ,aa
JUMP C,aa
JUMP NC,aa
CALL aa
CALL Z,aa
CALL NZ,aa
CALL C,aa
CALL NC,aa
RET
RET Z
RET NZ
RET C
RET NC

Shift and Rotate Group

SR0 sX
SR1 sX
SRX sX
SRA sX
RR sX
SL0 sX
SL1 sX
SLX sX
SLA sX
RL sX

Input/Output Group

IN sX,pp
IN sX,(sY)
OUT sX,pp
OUT sX,(sY)

Interrupt Group

RETI ENABLE
RETI DISABLE
EINT
DINT

Logical Group

LOAD sX,kk
AND sX,kk
OR sX,kk
XOR sX,kk
LOAD sX,sY
AND sX,sY
OR sX,sY
XOR sX,sY
COMP sX,kk

Arithmetic Group

ADD sX,kk
ADDC sX,kk
SUB sX,kk
SUBC sX,kk
ADD sX,sY
ADDC sX,sY
SUB sX,sY
SUBC sX,sY

Note:

“X” and “Y” refer to storage registers “s” in range 0 to F.
“kk” represents a constant, range 00 to FF.
“aa” represents an address, range 00 to FF.
“pp” represents a data address, range 00 to FF.
Maximum Call and Return stack depth is 15.